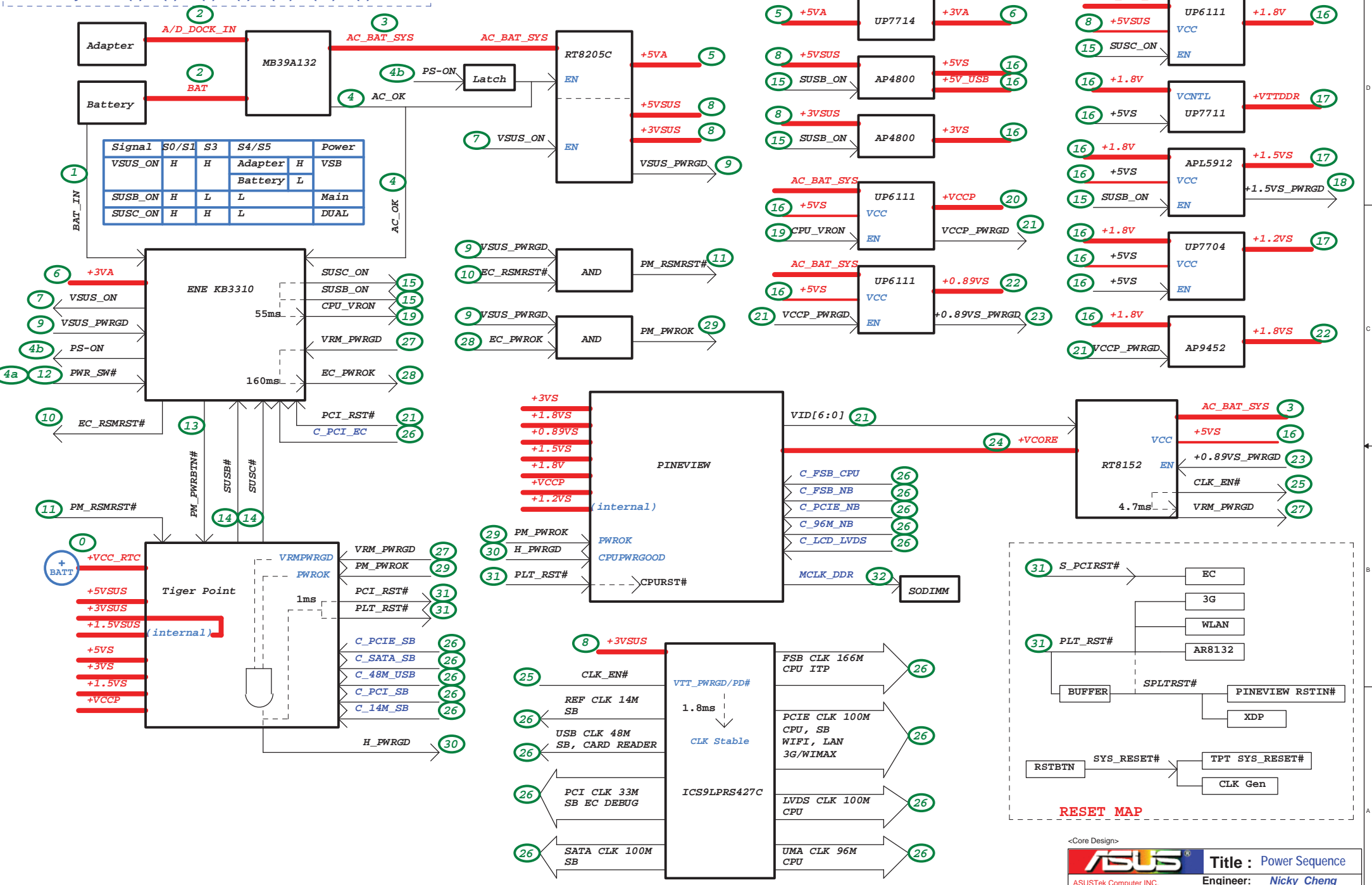
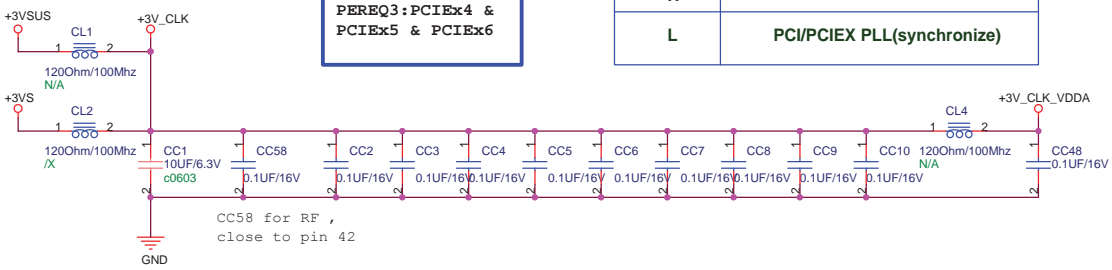
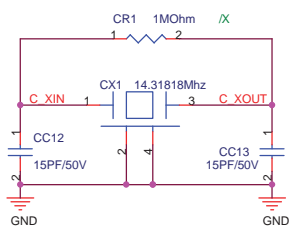


For Adapter Mode: (1) -> (2) -> (3) -> (4) -> (5) -> ...
 For Battery Mode: (1) -> (2) -> (3) -> (4) -> (4a) -> (4b) -> (5) -> ...



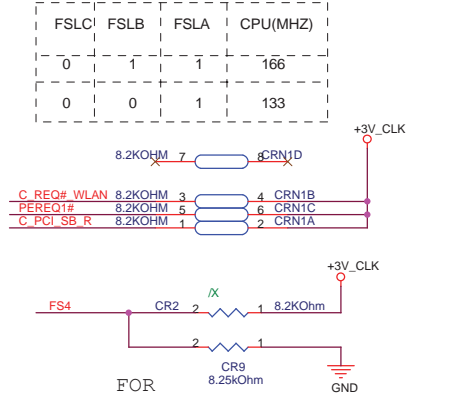
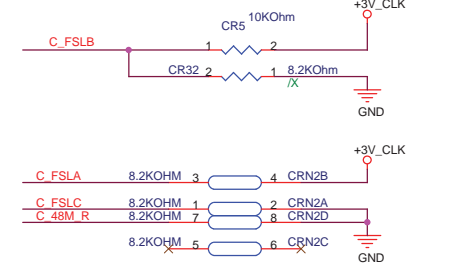
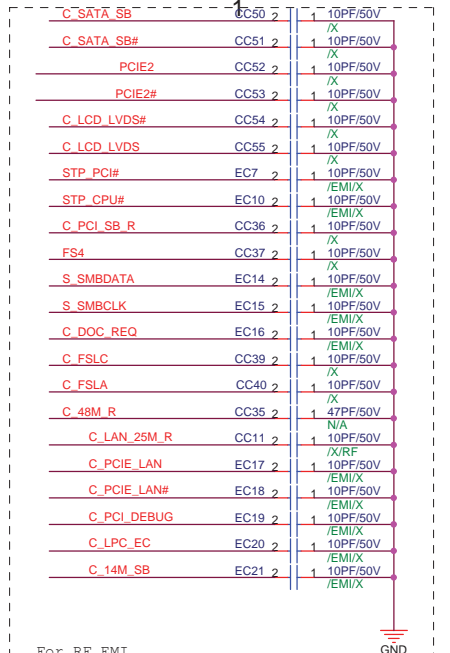
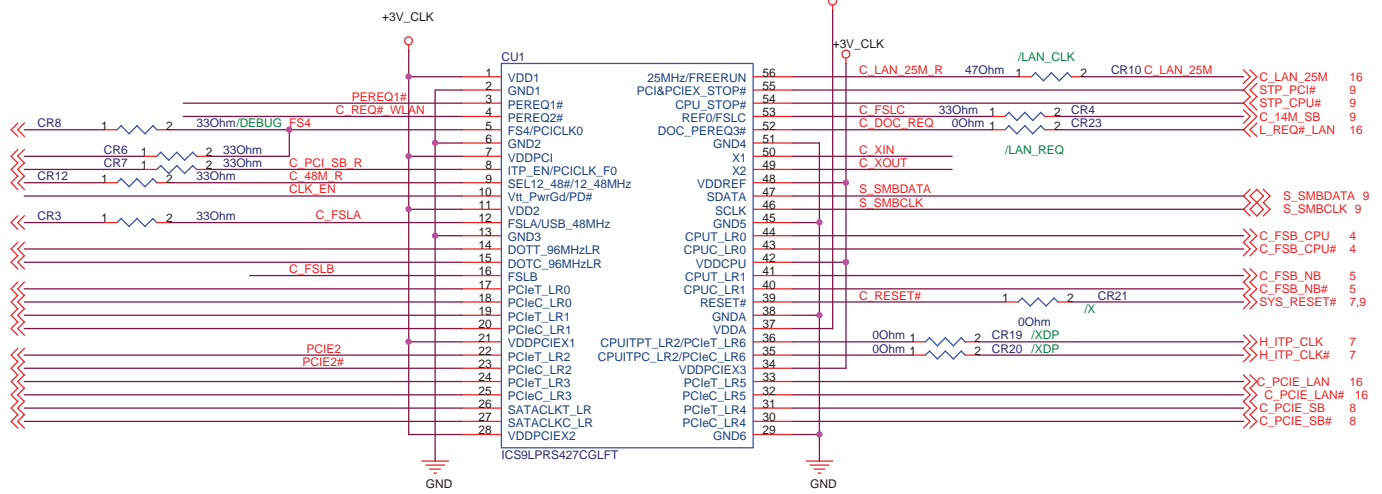


1:Disable
0:Enable

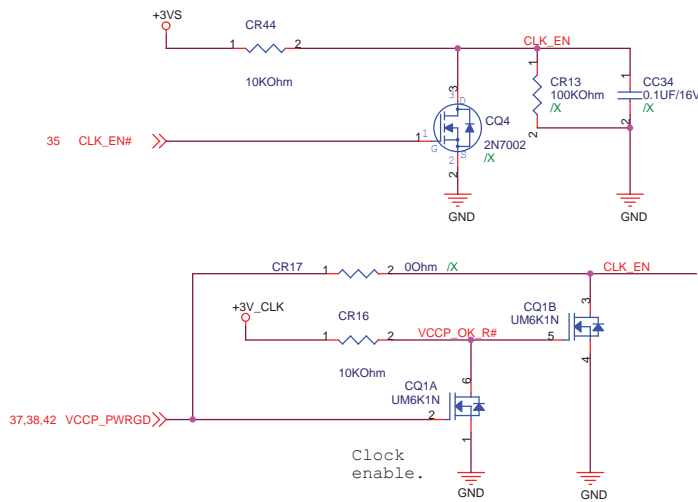
PEREQ1:PCIEx0 &
PCIEx1
PEREQ2:PCIEx2 &
PCIEx3 & SATA
PEREQ3:PCIEx4 &
PCIEx5 & PCIEx6

FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)

- 26 C_PCI_DEBUG
- 24 C_LPC_EC
- 28 C_48M_CARD_READER
- 8 C_48M_USB
- 5 C_96M_NB
- 5 C_96M_NB#
- 5 C_LCD_LVDS
- 5 C_LCD_LVDS#
- 4 C_PCIE_NB
- 4 C_PCIE_NB#
- 18 C_PCIE_WIMAX
- 18 C_PCIE_WIMAX#
- 17 C_PCIE_WLAN
- 17 C_PCIE_WLAN#
- 9 C_SATA_SB
- 9 C_SATA_SB#



O_DOC1	O_DOC2	Voltage	Status
L	L	2.4-3.3V	Super
L	H	0.5-2.36V	Normal
H	*	0-0.35V	Power saving



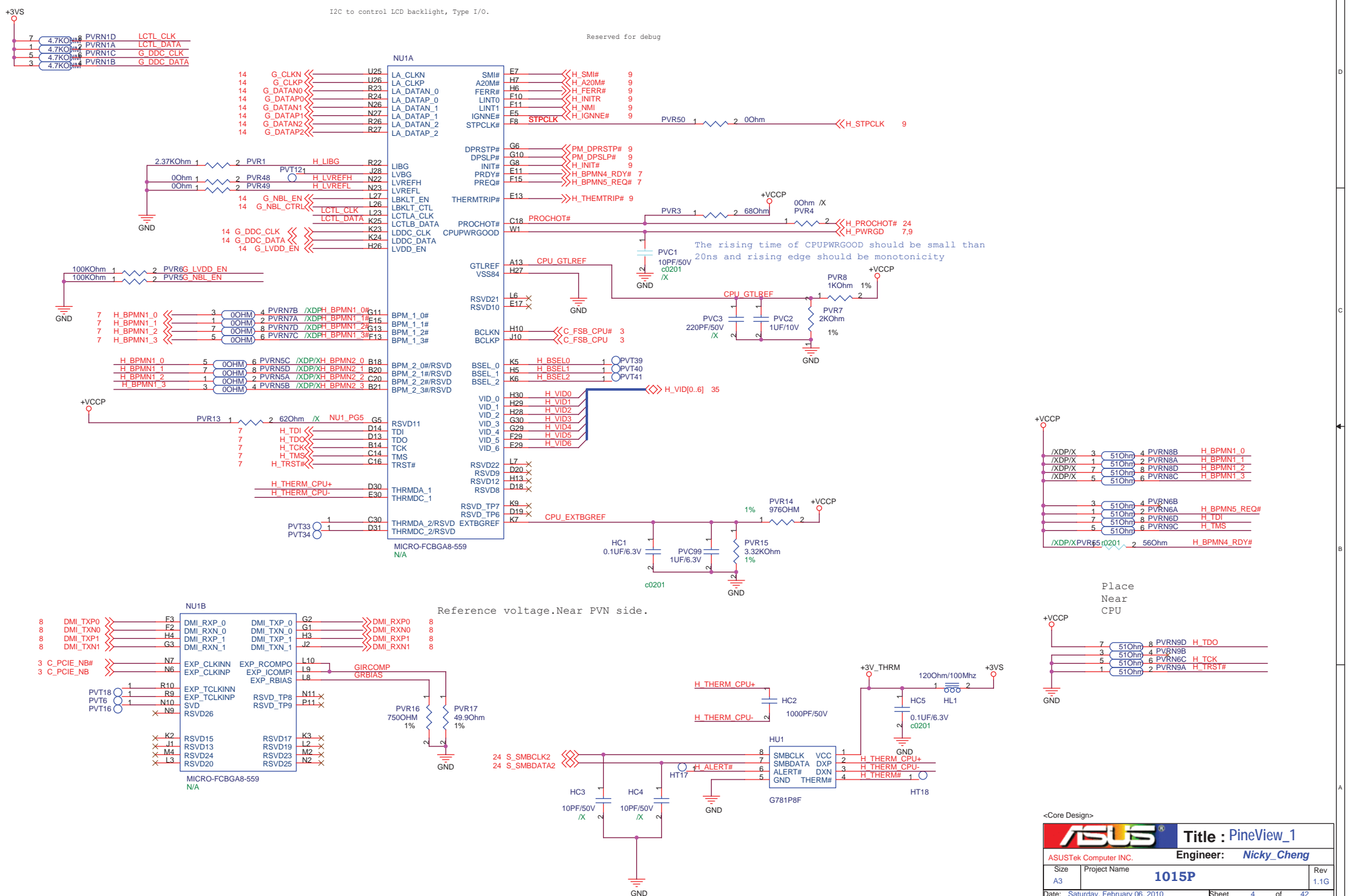
<Core Design>

ASUS Title: ICS9LPRS427C

ASUSTek Computer INC. Engineer: Nicky_Cheng

Size	Project Name	Rev
A3	1015P	1.1G

Date: Saturday, February 06, 2010 Sheet 3 of 42



11,12 D2_MAA[14:0] <<>

NU1C
 D2_MAA0 AH19
 D2_MAA1 AJ18
 D2_MAA2 AK18
 D2_MAA3 AK16
 D2_MAA4 AJ14
 D2_MAA5 AH14
 D2_MAA6 AK14
 D2_MAA7 AJ12
 D2_MAA8 AH13
 D2_MAA9 AK12
 D2_MAA10 AK20
 D2_MAA11 AH12
 D2_MAA12 AH12
 D2_MAA13 AJ24
 D2_MAA14 AJ10

11,12 D2_WEA# <<> AK22
 11,12 D2_CASA# <<> AJ22
 11,12 D2_RASA# <<> AK21

11,12 D2_BAA0 <<> AJ20
 11,12 D2_BAA1 <<> AH20
 11,12 D2_BAA2 <<> AK11

11,12 D2_CS_A#0 <<> AH22
 11,12 D2_CS_A#1 <<> AK25
 11,12 D2_CS_A#2 <<> AJ21
 11,12 D2_CS_A#3 <<> AJ25

11,12 D2_CKE_A0 <<> AH10
 11,12 D2_CKE_A1 <<> AH9
 11,12 D2_CKE_A2 <<> AK10
 11,12 D2_CKE_A3 <<> AJ8

11,12 D2_ODT_A0 <<> AK24
 11,12 D2_ODT_A1 <<> AH26
 11,12 D2_ODT_A2 <<> AH24
 11,12 D2_ODT_A3 <<> AK27

11 D2_MA_CLK0 <<> AG15
 11 D2_MA_CLK#0 <<> AF15
 11 D2_MA_CLK1 <<> AD13
 11 D2_MA_CLK#1 <<> AC13

AD15
 AD13
 AF13
 AG13

AD17
 AC17
 AB15
 AB17

RSVD5
 RSVD4
 RSVD1
 RSVD2

RSVD3
 RSVD7
 RSVD_TP4
 RSVD_TP5

RSVD6
 DDR_VREF
 DDR_RPD
 DDR_RPU

RSVD6
 DDR_A_DQS_5
 DDR_A_DM_5

RSVD6
 DDR_A_DQ_40
 DDR_A_DQ_41
 DDR_A_DQ_42
 DDR_A_DQ_43
 DDR_A_DQ_44
 DDR_A_DQ_45
 DDR_A_DQ_46
 DDR_A_DQ_47

DDR_A_DQS_6
 DDR_A_DQS#_6
 DDR_A_DM_6

DDR_A_DQ_48
 DDR_A_DQ_49
 DDR_A_DQ_50
 DDR_A_DQ_51
 DDR_A_DQ_52
 DDR_A_DQ_53
 DDR_A_DQ_54
 DDR_A_DQ_55

DDR_A_DQS_7
 DDR_A_DQS#_7
 DDR_A_DM_7

DDR_A_DQ_56
 DDR_A_DQ_57
 DDR_A_DQ_58
 DDR_A_DQ_59
 DDR_A_DQ_60
 DDR_A_DQ_61
 DDR_A_DQ_62
 DDR_A_DQ_63

DDR_A_DQS_0
 DDR_A_DQS#_0
 DDR_A_DM_0
 DDR_A_DQ_0
 DDR_A_DQ_1
 DDR_A_DQ_2
 DDR_A_DQ_3
 DDR_A_DQ_4
 DDR_A_DQ_5
 DDR_A_DQ_6
 DDR_A_DQ_7
 DDR_A_DQS_1
 DDR_A_DQS#_1
 DDR_A_DM_1
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 DDR_A_DQ_11
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 DDR_A_DQ_39

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DDR_A_DQ_32
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 DDR_A_DQ_99

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 DDR_A_DQ_98
 DDR_A_DQ_99

D2_DQ_A[63:0] 11
 D2_DQS_A[7:0] 11
 D2_DQS_A#[7:0] 11
 D2_DM_A[7:0] 11

XDP_RSVD5
 XDP_RSVD9
 XDP_RSVD11
 XDP_RSVD17

XDP_RSVD17
 XDP_RSVD18
 XDP_RSVD19
 XDP_RSVD20

XDP_RSVD20
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 XDP_RSVD19
 XDP_RSVD20

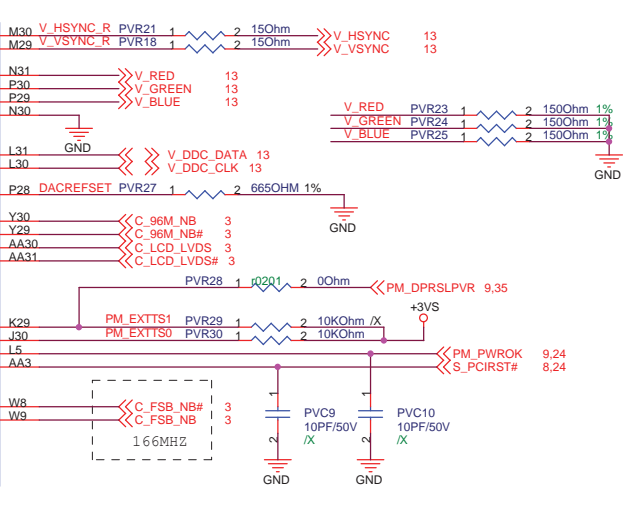
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 XDP_RSVD99

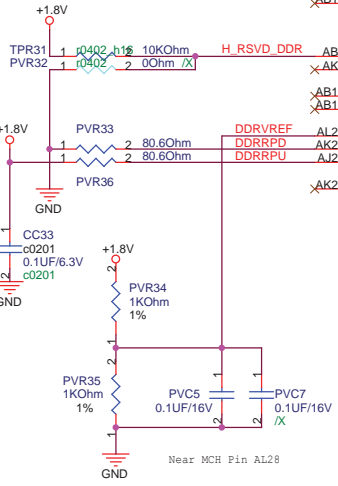
NU1D
 XDP_RSVD[0] CRT_HSYNC
 XDP_RSVD[1] CRT_VSYNC
 XDP_RSVD[2] CRT_RED
 XDP_RSVD[3] CRT_GREEN
 XDP_RSVD[4] CRT_BLUE
 XDP_RSVD[5] CRT_IRTN
 XDP_RSVD[6] CRT_DDC_DATA
 XDP_RSVD[7] CRT_DDC_CLK
 XDP_RSVD[8] DAC_IREF
 XDP_RSVD[9] REFCLKINP
 XDP_RSVD[10] REFCLKINN
 XDP_RSVD[11] REFSSCLKINP
 XDP_RSVD[12] REFSSCLKINN
 XDP_RSVD[13] HPL_CLKINN
 XDP_RSVD[14] HPL_CLKINP
 XDP_RSVD[15] RSVD_TP3
 XDP_RSVD[16] RSVD_TP2
 XDP_RSVD[17] RSVD_TP10
 XDP_RSVD[18] RSVD_TP11
 XDP_RSVD[19] RSVD_TP1
 XDP_RSVD[20] RSVD_TP14
 XDP_RSVD[21] RSVD_TP12
 XDP_RSVD[22] RSVD_TP13



DDC CLK&DATA need 2.2K Pull up to +3VS(Or may we can use 4.7K);connector side has pull-up resistor.

CPU Sample SKU	ASUS P/N
ES1	01G013070000
ES2	01G0132000000
QS	01G0132000001
PRQ	01G0132000002

Intel confirm only RSVD9 need stuff 1K resistor.



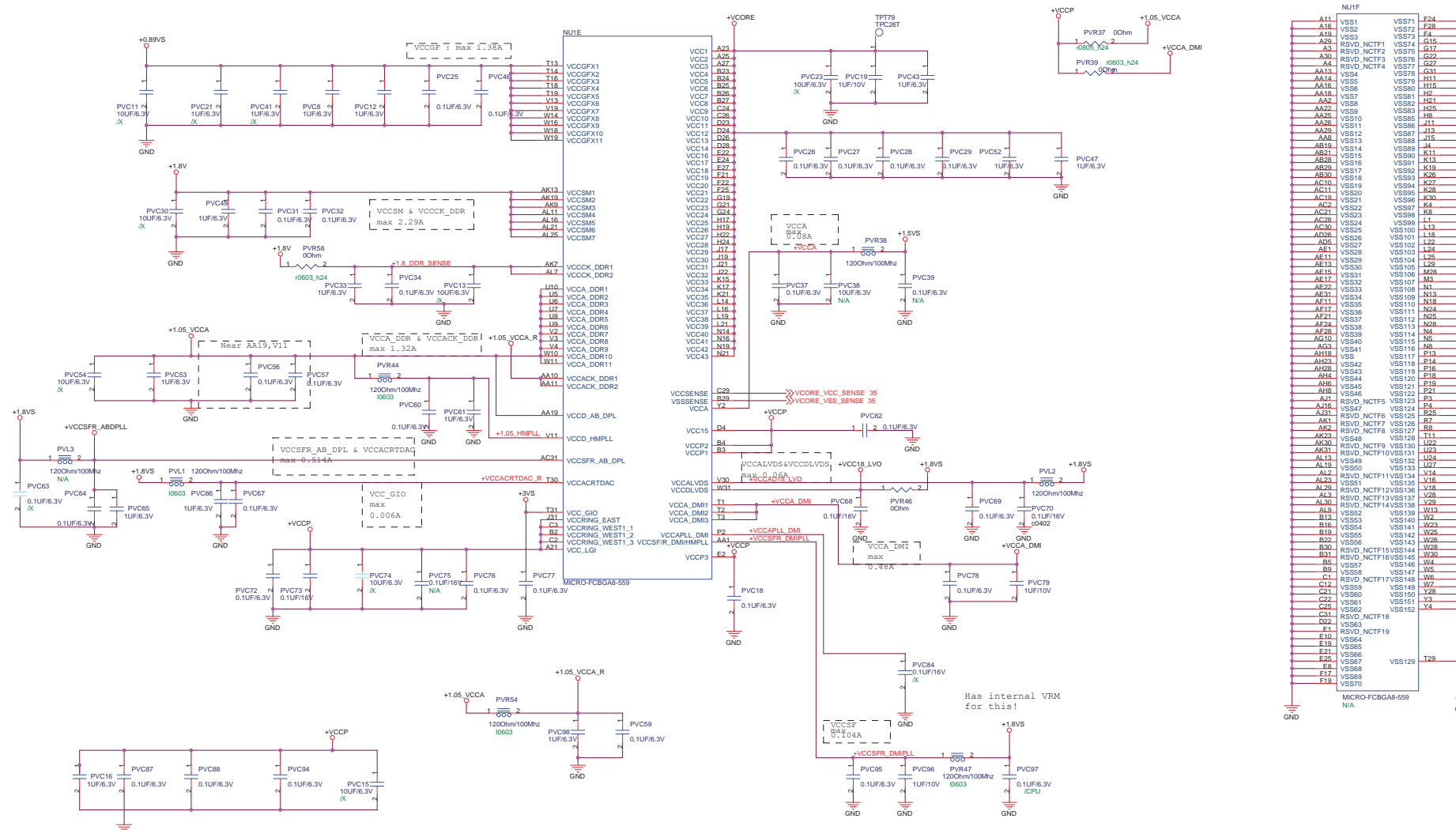
<Core Design>

ASUS Title : PineView_2

ASUSTek Computer INC. Engineer: Nicky Cheng

Size	Project Name	Rev
A3	1015P	1.0G

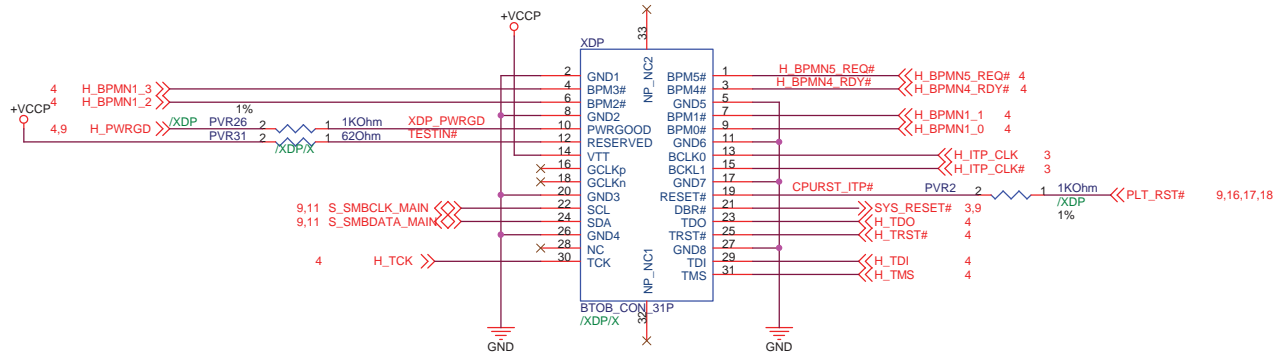
Date: Saturday, February 06, 2010 Sheet 5 of 42



VCC = 3.5A
 VCCA = 0.08A
 VCCGFX = 1.38A
 VCCALVDS , VCCDLVDS = 0.06A
 VCCA_DMI = 0.48A
 VCCSFR_DMIHMPLL = 0.104A
 VCCA_DDR and VCCACK_DDR = 1.32A
 VCCSM and VCCCK_DDR = 2.27A
 VCCRING_EAST , VCCRING_EAST_WEST , VCC_LGI , VCCD_AB_DPL , VCCD_HMPLL = 0.33A
 VCC_GIO = 0.006A
 VCCSFR_AB_DPL , VCCACRTDAC = 0.154A

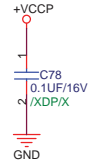
Current for PineView

NU1F		
A11	VSS1	VSS71
A16	VSS2	VSS72
A19	VSS3	VSS73
A28	RSVD_NCTF1	VSS74
A31	RSVD_NCTF2	VSS75
A30	RSVD_NCTF3	VSS76
A4	RSVD_NCTF4	VSS77
AA13	VSS4	VSS78
AA16	VSS5	VSS79
AA25	VSS6	VSS80
AA8	VSS7	VSS81
AA2	VSS8	VSS82
AA25	VSS9	VSS83
AA25	VSS10	VSS84
AA25	VSS11	VSS85
AA29	VSS12	VSS86
AA8	VSS13	VSS87
AB19	VSS14	VSS88
AB21	VSS15	VSS89
AB28	VSS16	VSS90
AB29	VSS17	VSS91
AB30	VSS18	VSS92
AC10	VSS19	VSS93
AC19	VSS20	VSS94
AC2	VSS21	VSS95
AC41	VSS22	VSS96
AC28	VSS23	VSS97
AD26	VSS24	VSS98
AD26	VSS25	VSS99
AD5	VSS26	VSS100
AE1	VSS27	VSS101
AE11	VSS28	VSS102
AE13	VSS29	VSS103
AE15	VSS30	VSS104
AE17	VSS31	VSS105
AE22	VSS32	VSS106
AE31	VSS33	VSS107
AE31	VSS34	VSS108
AE37	VSS35	VSS109
AE37	VSS36	VSS110
AF21	VSS37	VSS111
AF24	VSS38	VSS112
AF28	VSS39	VSS113
AG10	VSS40	VSS114
AG3	VSS41	VSS115
AH23	VSS42	VSS116
AH23	VSS43	VSS117
AH28	VSS44	VSS118
AH4	VSS45	VSS119
AH6	VSS46	VSS120
AH6	VSS47	VSS121
AH6	VSS48	VSS122
AJ1	RSVD_NCTF5	VSS123
AJ16	VSS49	VSS124
AK1	RSVD_NCTF6	VSS125
AK2	RSVD_NCTF7	VSS126
AK2	RSVD_NCTF8	VSS127
AK3	VSS48	VSS128
AK30	RSVD_NCTF9	VSS129
AK31	RSVD_NCTF10	VSS130
AL13	VSS49	VSS131
AL19	VSS50	VSS132
AL2	VSS50	VSS133
AL24	RSVD_NCTF11	VSS134
AL24	VSS51	VSS135
AL28	RSVD_NCTF12	VSS136
AL30	RSVD_NCTF13	VSS137
AL9	RSVD_NCTF14	VSS138
B13	VSS52	VSS139
B16	VSS53	VSS140
B16	VSS54	VSS141
B19	VSS55	VSS142
B22	VSS56	VSS143
B30	RSVD_NCTF15	VSS144
B5	RSVD_NCTF16	VSS145
B5	VSS57	VSS146
B9	VSS58	VSS147
C11	RSVD_NCTF17	VSS148
C12	VSS59	VSS149
C21	VSS60	VSS150
C22	VSS60	VSS150
C25	VSS62	VSS152
C31	RSVD_NCTF18	VSS151
D22	VSS63	VSS152
E1	RSVD_NCTF19	VSS153
E10	VSS64	VSS154
E19	VSS65	VSS155
E41	VSS66	VSS156
E25	VSS67	VSS157
F8	VSS68	VSS158
F17	VSS69	VSS159
F19	VSS70	VSS160
F24	VSS71	VSS161
F28	VSS72	VSS162
F4	VSS73	VSS163
G15	VSS74	VSS164
G17	VSS75	VSS165
G22	VSS76	VSS166
G27	VSS77	VSS167
G31	VSS78	VSS168
H11	VSS79	VSS169
H15	VSS80	VSS170
H21	VSS81	VSS171
H21	VSS82	VSS172
H25	VSS83	VSS173
H25	VSS84	VSS174
H25	VSS85	VSS175
H25	VSS86	VSS176
H25	VSS87	VSS177
H25	VSS88	VSS178
H25	VSS89	VSS179
H25	VSS90	VSS180
H25	VSS91	VSS181
H25	VSS92	VSS182
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H25	VSS120	VSS210
H25	VSS121	VSS211
H25	VSS122	VSS212
H25	VSS123	VSS213
H25	VSS124	VSS214
H25	VSS125	VSS215
H25	VSS126	VSS216
H25	VSS127	VSS217
H25	VSS128	VSS218
H25	VSS129	VSS219
H25	VSS130	VSS220
H25	VSS131	VSS221
H25	VSS132	VSS222
H25	VSS133	VSS223
H25	VSS134	VSS224
H25	VSS135	VSS225
H25	VSS136	VSS226
H25	VSS137	VSS227
H25	VSS138	VSS228
H25	VSS139	VSS229
H25	VSS140	VSS230
H25	VSS141	VSS231
H25	VSS142	VSS232
H25	VSS143	VSS233
H25	VSS144	VSS234
H25	VSS145	VSS235
H25	VSS146	VSS236
H25	VSS147	VSS237
H25	VSS148	VSS238
H25	VSS149	VSS239
H25	VSS150	VSS240
H25	VSS151	VSS241
H25	VSS152	VSS242
H25	VSS153	VSS243
H25	VSS154	VSS244
H25	VSS155	VSS245
H25	VSS156	VSS246
H25	VSS157	VSS247
H25	VSS158	VSS248
H25	VSS159	VSS249
H25	VSS160	VSS250



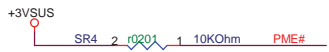
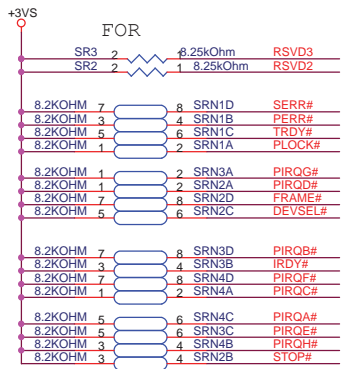
Change Device and PCB footprint of XDP1 to nomask footprint - nomask solution

糧 Layout 缺贺叫 XDP Connector 叫確 12G161300311 (w/ 2 through holes)

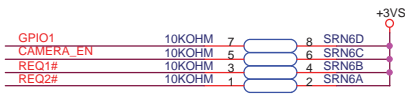
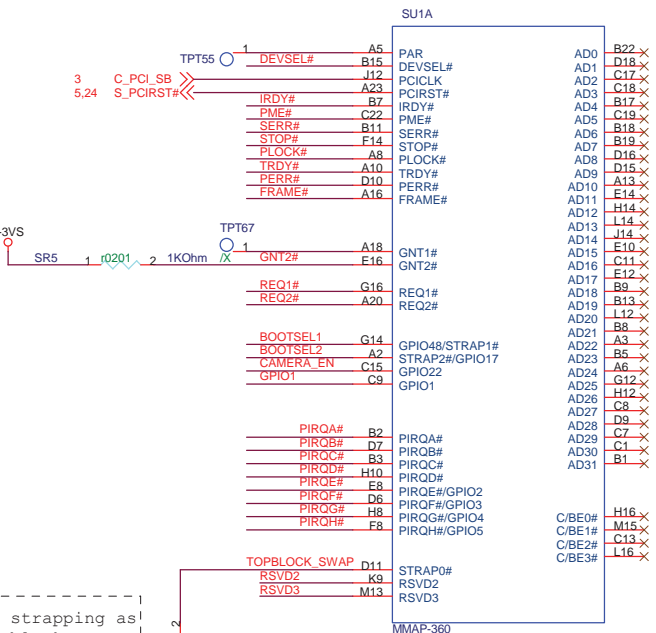


<Core Design>

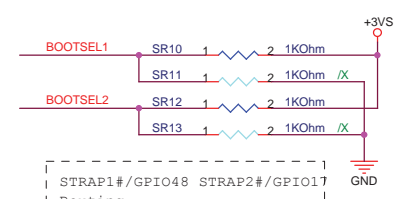
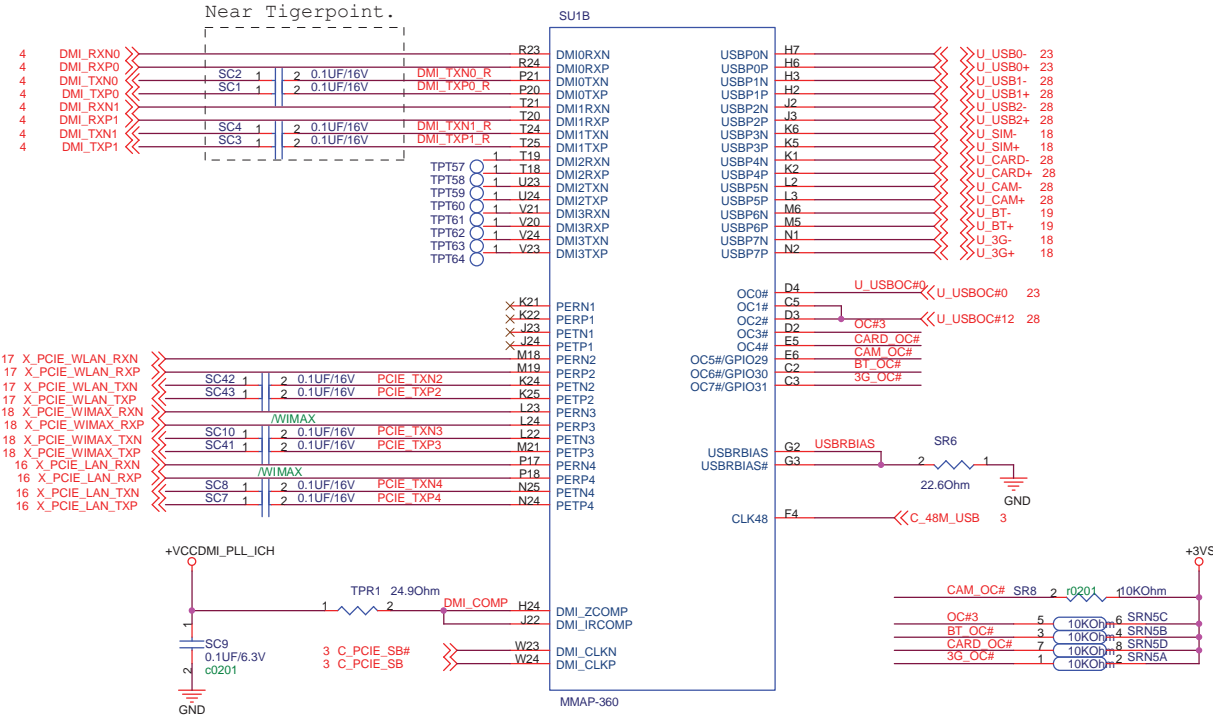
ASUS		Title : XDP	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size A3	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 7 of 42	



Remain
PCICLK

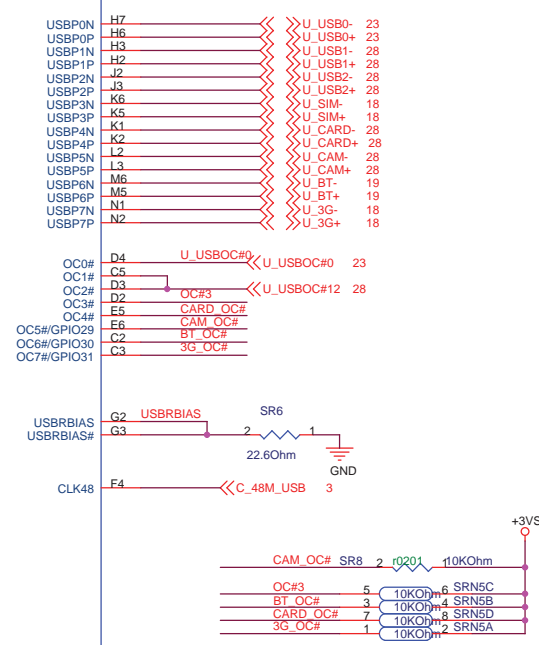


For strapping as
Top-block Swap
override.



STRAP1#/GPIO48 STRAP2#/GPIO17
 Routing
 0 1: Flash Cycles Routed to SPI
 1 0: Flash Cycles Routed to PCI
 1 1: Flash Cycles Routed to LPC

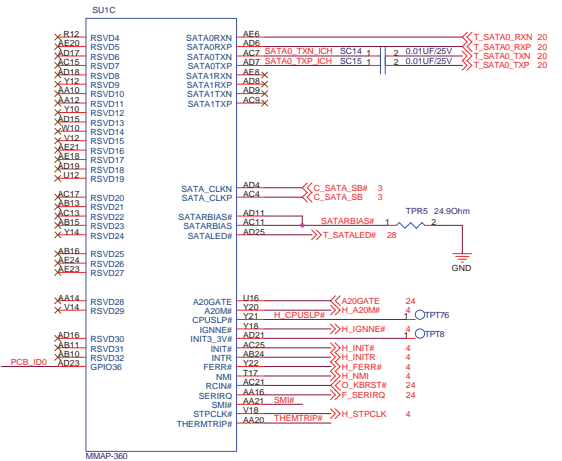
USB0	USB CONN
USB1	USB CONN
USB2	USB CONN
USB3	USIM
USB4	Card Reader
USB5	Camera
USB6	Blue tooth
USB7	3G



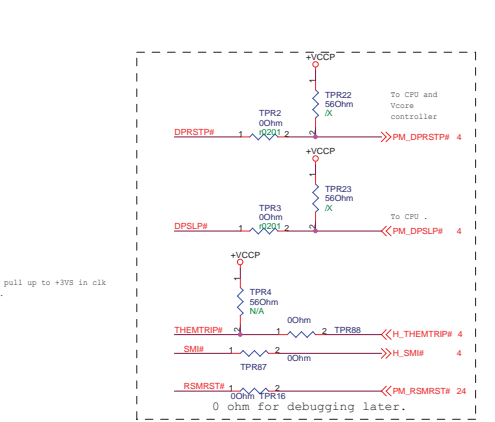
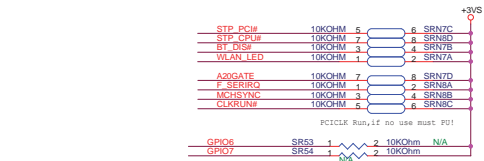
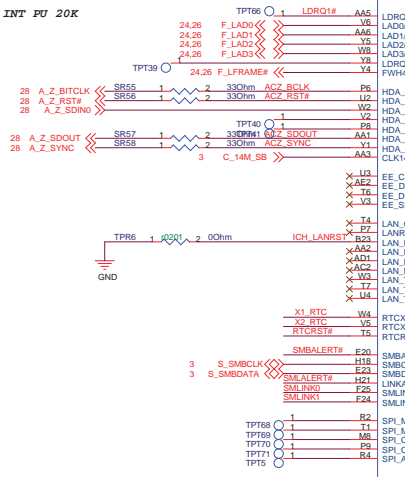
CLK 14MHZ has a 22ohm resistor near clk Gen.

LDRQ0/1 LPC DMA/master request, ICH7M has internal PU, but we need TPT datasheet

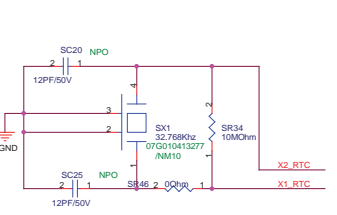
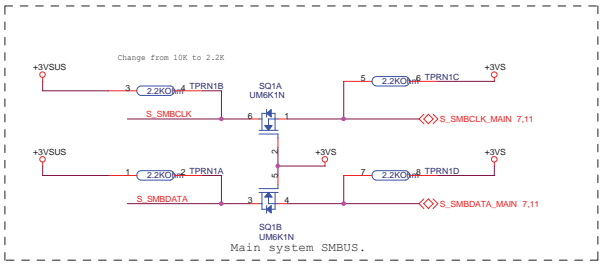
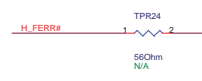
SATA RX, TX all need AC couple and place near Connector side for signal quality. And Traces to them should match length. ICH7M need pull down RX, if no use.



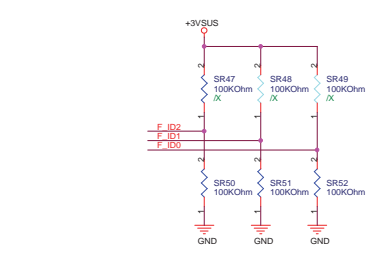
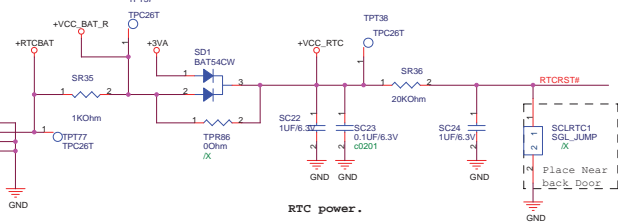
LAD[0:3] INT PU 20K



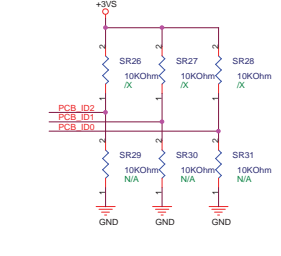
SB Sample SKU	ASUS P/N
QS	02G010026301
PRQ	02G010026302



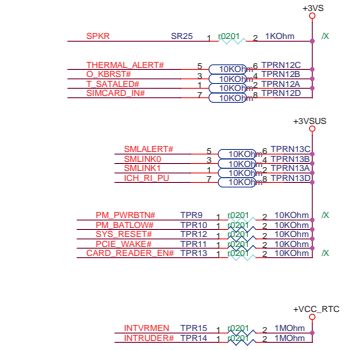
S BATT



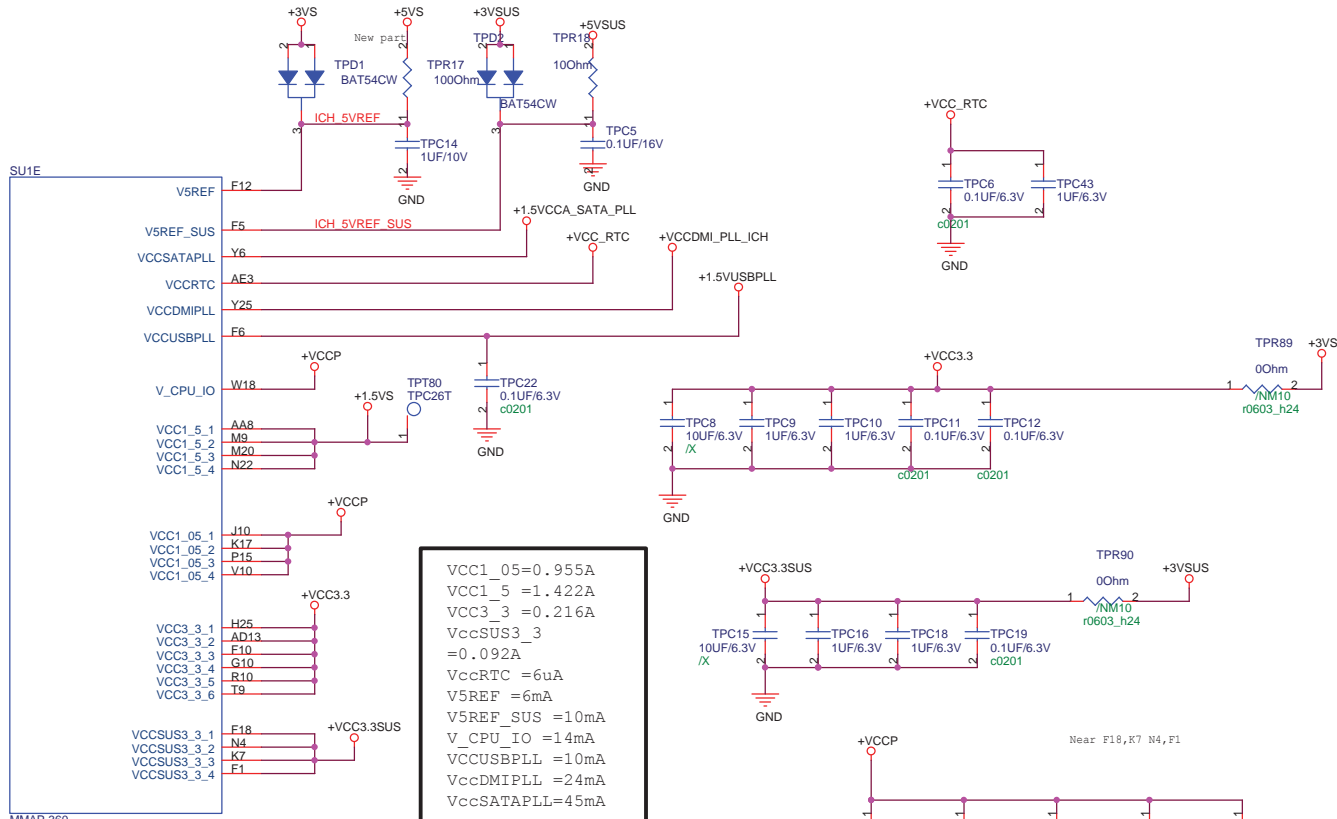
RTC well input requires pull down to reduce leakage from coin cell battery in G3. Can't float in G3.



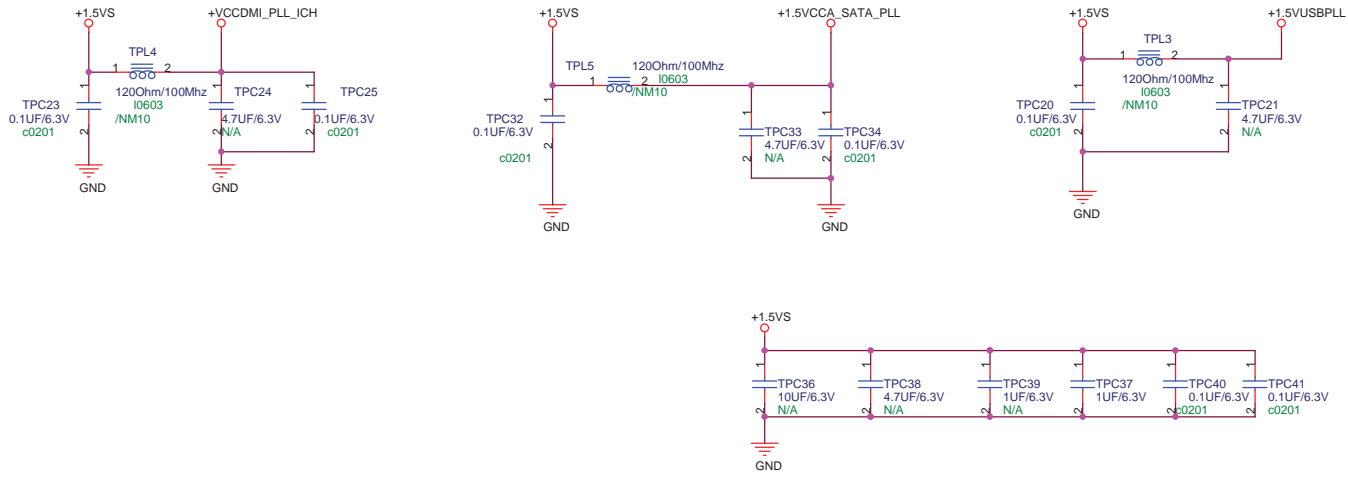
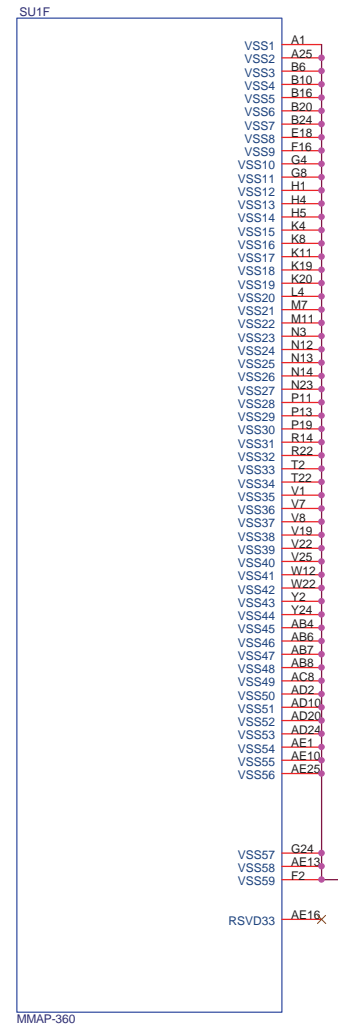
1=DMI interface is strapped to operate in DC coupled mode. 0=DMI interface is strapped to operate in AC coupled mode.



For Rechargeable solution: Mount TPR2
For NON-Rechargeable solution: Unmount TPR2



VCC1_05=0.955A
 VCC1_5 =1.422A
 VCC3_3 =0.216A
 VccSUS3_3
 =0.092A
 VccRTC =6uA
 V5REF =6mA
 V5REF_SUS =10mA
 V_CPU_IO =14mA
 VCCUSBPLL =10mA
 VccDMIPLL =24mA
 VccSATAPLL=45mA

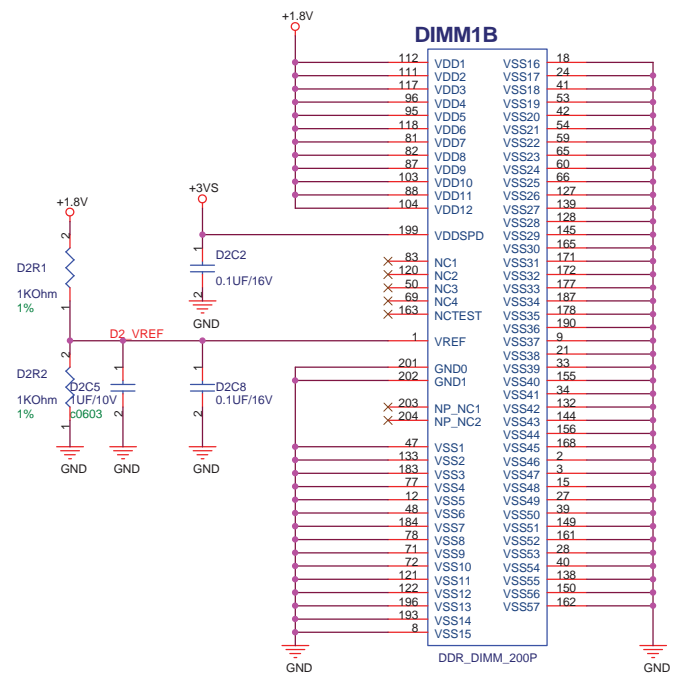
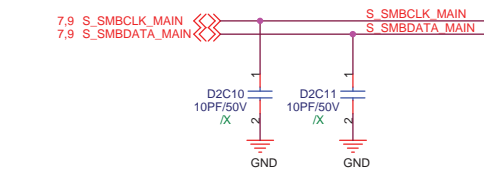


<< >>D2_DQ_A[63:0] 5
 << >>D2_DQS_A[7:0] 5
 << >>D2_DQS_A#[7:0] 5
 << >>D2_DM_A[7:0] 5
 << >>D2_MAA[14:0] 5,12

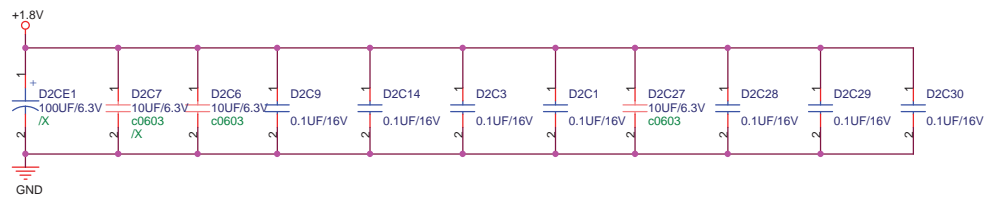
DIMM1A

D2_MAA0	102	A0	DQ0	5	D2_DQ_A0
D2_MAA1	101	A1	DQ1	7	D2_DQ_A1
D2_MAA2	100	A2	DQ2	17	D2_DQ_A2
D2_MAA3	99	A3	DQ3	19	D2_DQ_A3
D2_MAA4	98	A4	DQ4	4	D2_DQ_A4
D2_MAA5	97	A5	DQ5	6	D2_DQ_A5
D2_MAA6	94	A6	DQ6	14	D2_DQ_A6
D2_MAA7	92	A6	DQ6	16	D2_DQ_A7
D2_MAA8	93	A7	DQ7	23	D2_DQ_A8
D2_MAA9	91	A8	DQ8	25	D2_DQ_A9
D2_MAA10	105	A10/AP	DQ10	35	D2_DQ_A10
D2_MAA11	80	A11	DQ11	37	D2_DQ_A11
D2_MAA12	89	A12	DQ12	20	D2_DQ_A12
D2_MAA13	116	A13	DQ13	22	D2_DQ_A13
D2_MAA14	86	A14	DQ14	36	D2_DQ_A14
	84	A15	DQ15	38	D2_DQ_A15
	85	A16_BA2	DQ16	43	D2_DQ_A16
			DQ17	45	D2_DQ_A17
			DQ18	57	D2_DQ_A18
			DQ19	44	D2_DQ_A19
			DQ20	20	D2_DQ_A20
			DQ21	46	D2_DQ_A21
			DQ22	56	D2_DQ_A22
			DQ23	58	D2_DQ_A23
			DQ24	61	D2_DQ_A24
			DQ25	63	D2_DQ_A25
			DQ26	73	D2_DQ_A26
			DQ27	75	D2_DQ_A27
			DQ28	62	D2_DQ_A28
			DQ29	64	D2_DQ_A29
			DQ30	74	D2_DQ_A30
			DQ31	76	D2_DQ_A31
			DQ32	123	D2_DQ_A32
			DQ33	125	D2_DQ_A33
			DQ34	135	D2_DQ_A34
			DQ35	137	D2_DQ_A35
			DQ36	124	D2_DQ_A36
			DQ37	126	D2_DQ_A37
			DQ38	134	D2_DQ_A38
			DQ39	136	D2_DQ_A39
			DQ40	141	D2_DQ_A40
			DQ41	143	D2_DQ_A41
			DQ42	151	D2_DQ_A42
			DQ43	153	D2_DQ_A43
			DQ44	140	D2_DQ_A44
			DQ45	142	D2_DQ_A45
			DQ46	152	D2_DQ_A46
			DQ47	154	D2_DQ_A47
			DQ48	157	D2_DQ_A48
			DQ49	159	D2_DQ_A49
			DQ50	173	D2_DQ_A50
			DQ51	175	D2_DQ_A51
			DQ52	158	D2_DQ_A52
			DQ53	160	D2_DQ_A53
			DQ54	174	D2_DQ_A54
			DQ55	176	D2_DQ_A55
			DQ56	179	D2_DQ_A56
			DQ57	181	D2_DQ_A57
			DQ58	189	D2_DQ_A58
			DQ59	191	D2_DQ_A59
			DQ60	180	D2_DQ_A60
			DQ61	182	D2_DQ_A61
			DQ62	192	D2_DQ_A62
			DQ63	194	D2_DQ_A63

DDR_DIMM_200P



"糧 Layout 訣賀叫σ祇2nd source / 12G025C2200X PCB footprint
 , 磷 2nd DIMM 斂耗婉築ノ玻ネ 豊- 2nd source PCB footprint
 數main source size DIMM羅 Tトイ"



<Core Design>

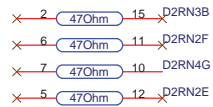
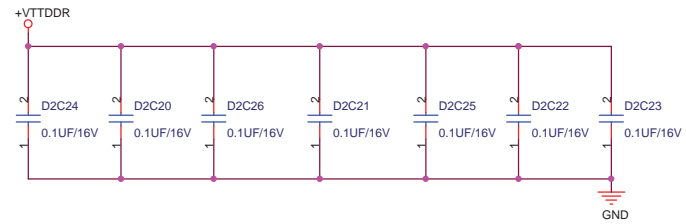
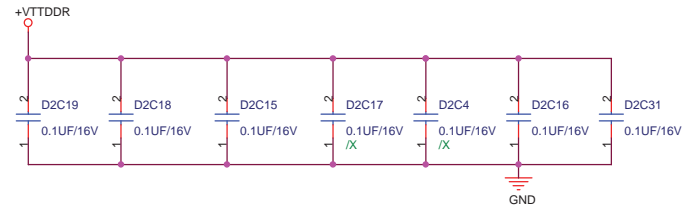
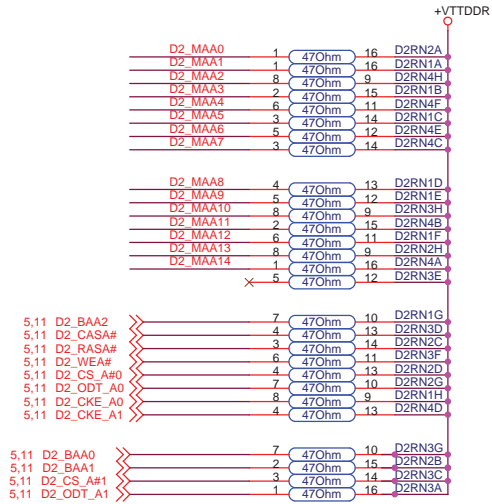
ASUS Title : **DDR2-SO-DIMM**

ASUSTek Computer INC. Engineer: **Nicky_Cheng**

Size	Project Name	Rev
A3	1015P	1.0G

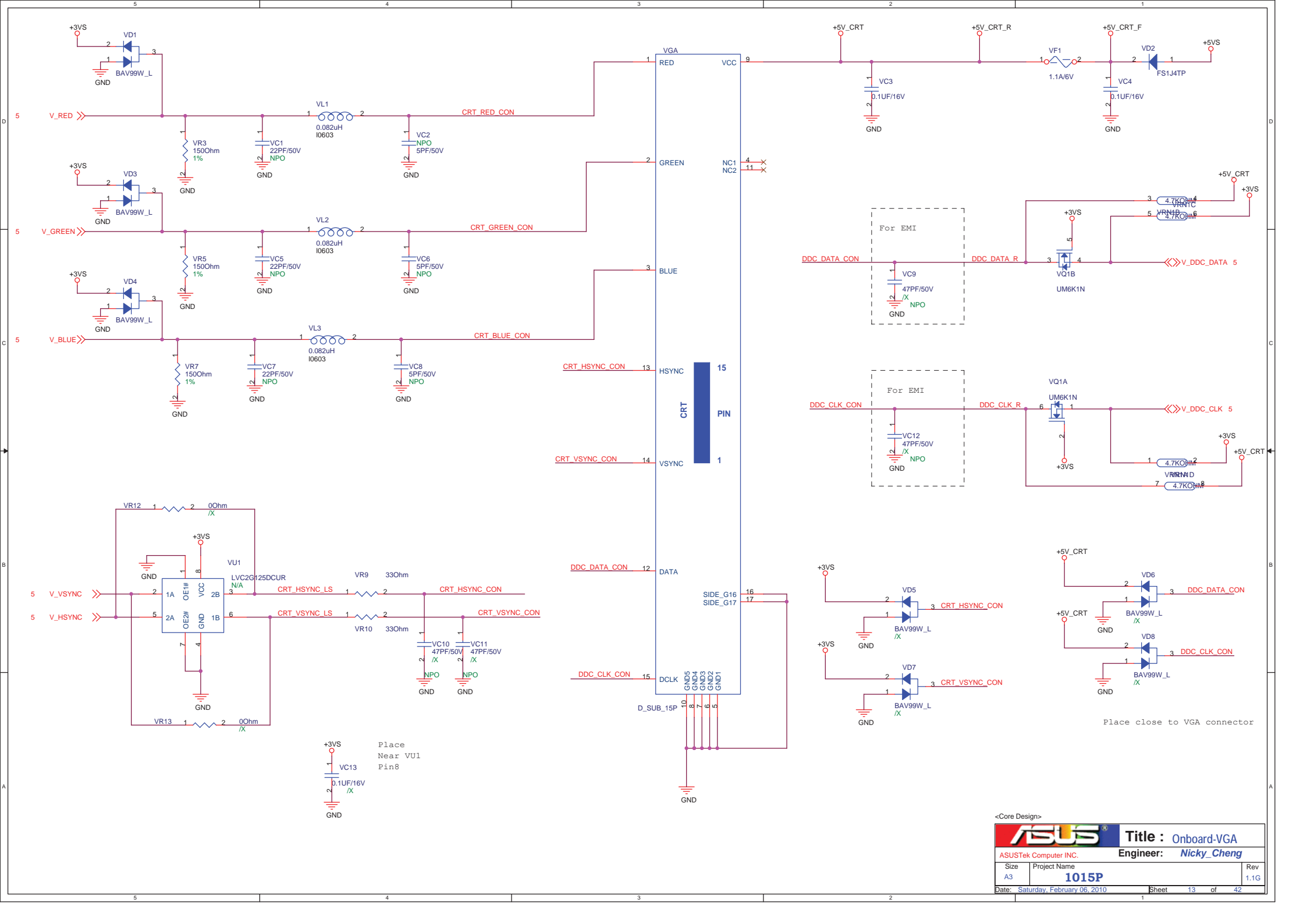
Date: Saturday, February 06, 2010 Sheet 11 of 42

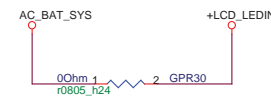
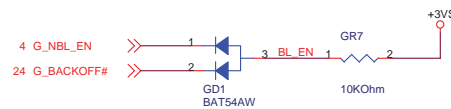
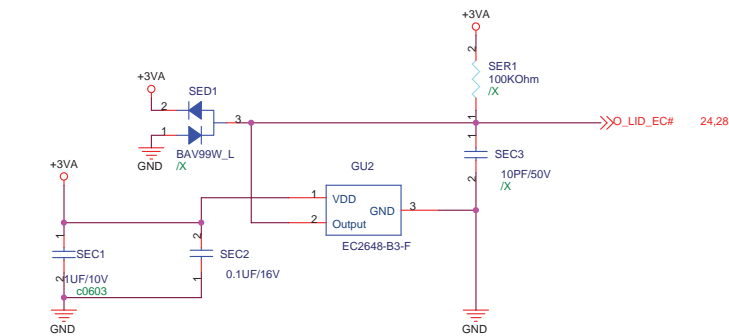
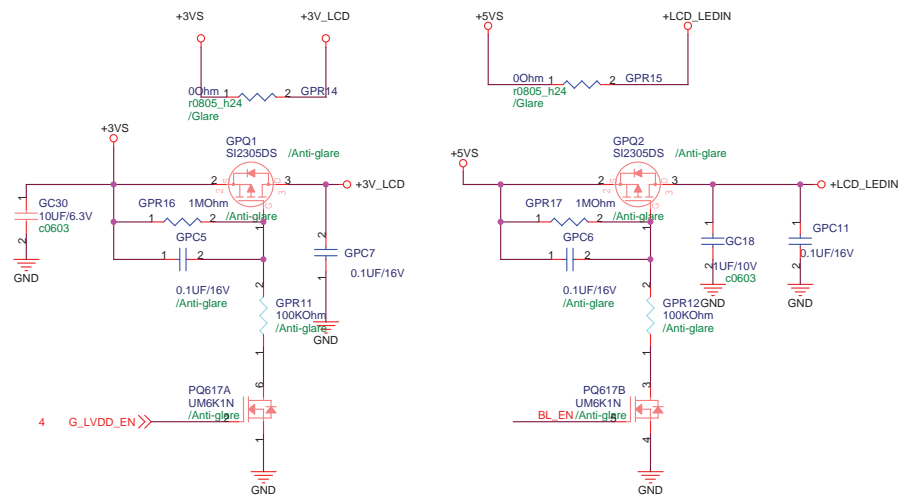
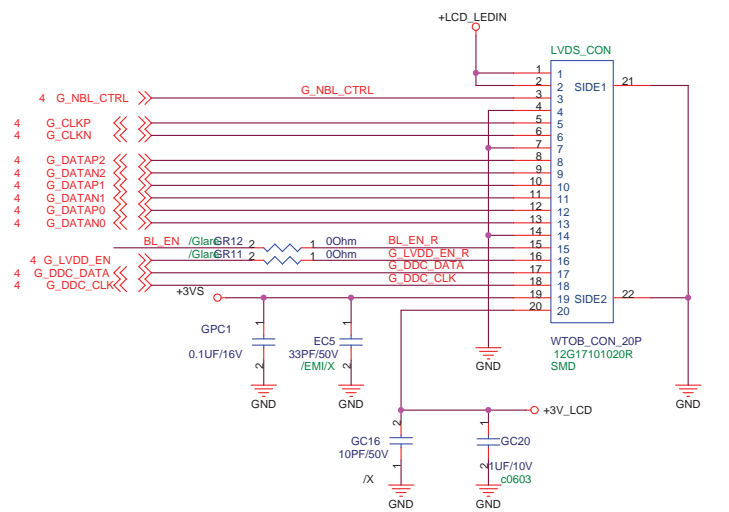
<< D2_MAA[14:0] 5,11



<Core Design>

ASUS		Title : DDR2-Termination	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size	Project Name	Rev	
A3	1015P	1.0G	
Date: Saturday, February 06, 2010		Sheet 12 of 42	

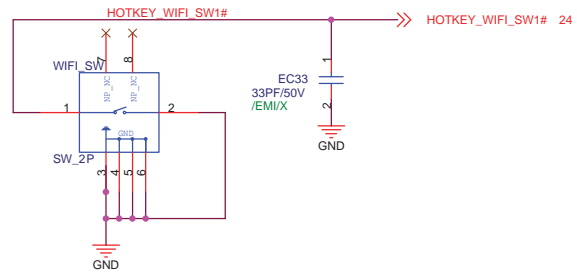
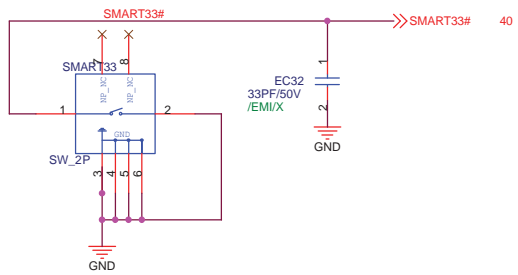




G_DDC_CLK	GC1	2	1	10PF/50V	/X
G_DDC_DATA	GC2	2	1	10PF/50V	/X
G_CLKP	GC3	2	1	10PF/50V	N/A
G_CLKN	GC4	2	1	10PF/50V	N/A
G_DATAP2	GC5	2	1	10PF/50V	N/A
G_DATAN2	GC6	2	1	10PF/50V	N/A
G_DATAP1	GC7	2	1	10PF/50V	N/A
G_DATAN1	GC8	2	1	10PF/50V	N/A
G_DATAP0	GC9	2	1	10PF/50V	N/A
G_DATAN0	GC10	2	1	10PF/50V	N/A
G_NBL_CTRL	GC12	2	1	10PF/50V	/X
BL_EN	EC11	2	1	10PF/50V	EMI/X
G_LVDD_EN	EC12	2	1	10PF/50V	EMI/X

<Core Design>

		Title : LVDS Conn_LID	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size	Project Name	Rev	
Custom	1015P	1.1G	
Date: Saturday, February 06, 2010		Sheet	14 of 42

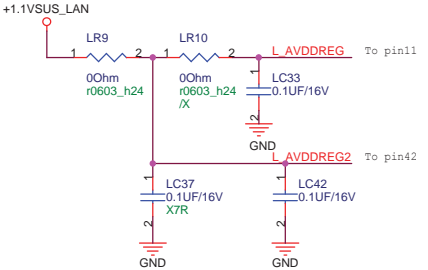
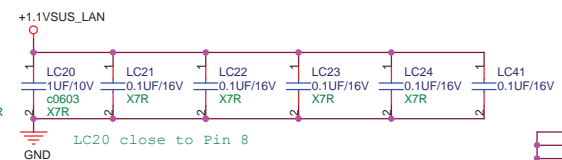
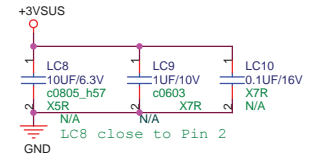
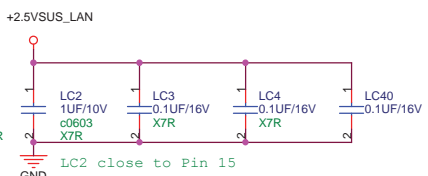


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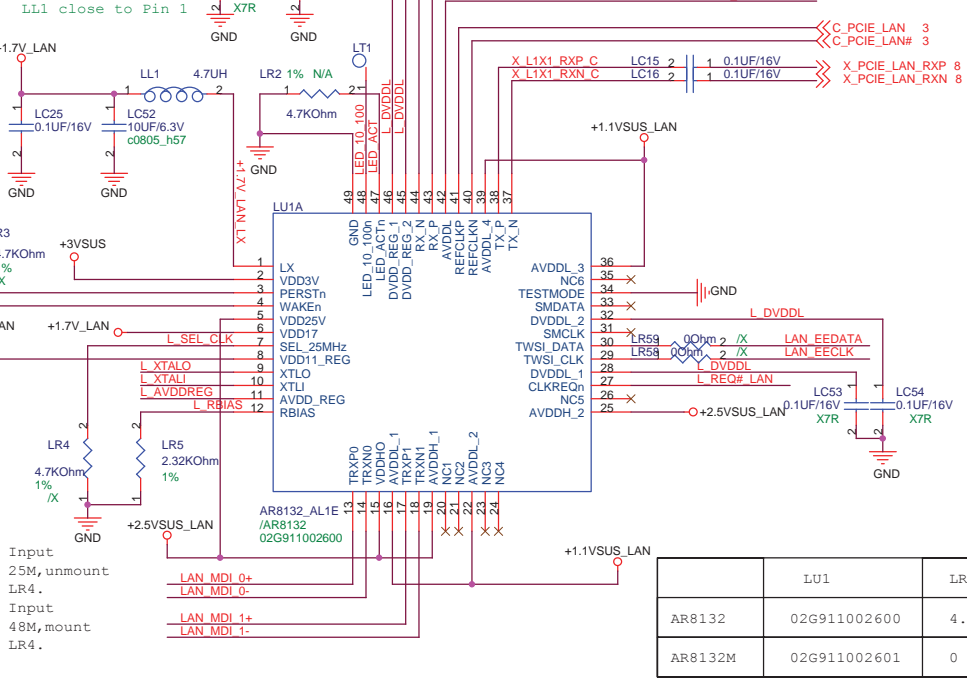
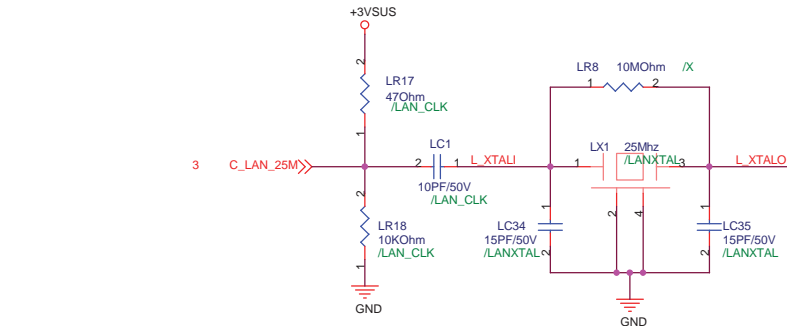
		Title : WIFI_SAMRT33
ASUSTek Computer INC.		Engineer: Nicky_Cheng
Size A3	Project Name 1015P	Rev 1.1G
Date: Saturday, February 06, 2010		Sheet 15 of 42

LAN AR8132M
Symbol 02G911002600
BOM 02G911002601

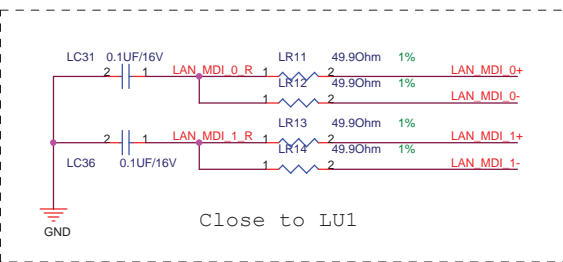
	LR2
Normal	N/A
Overclocking	/X



	LR9	LR10
Normal	N/A	/X
Overclocking	/X	N/A



	LU1	LR59	LR58	LC51	LU2	LC49	LC50
AR8132	02G911002600	4.7K	N/A	N/A	N/A	/X	/X
AR8132M	02G911002601	0 ohm	/X	/X	/X	/X	N/A



<Core Design>

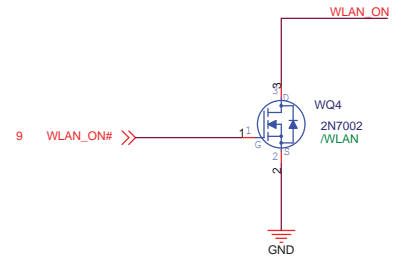
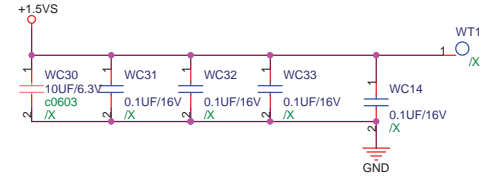
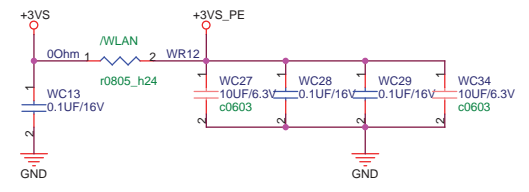
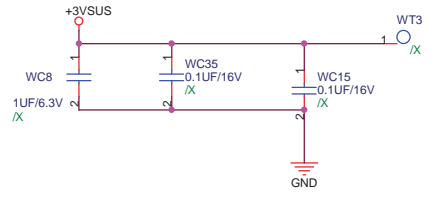
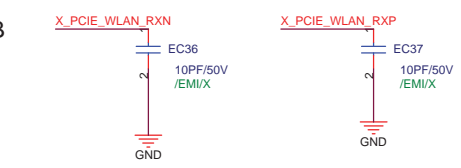
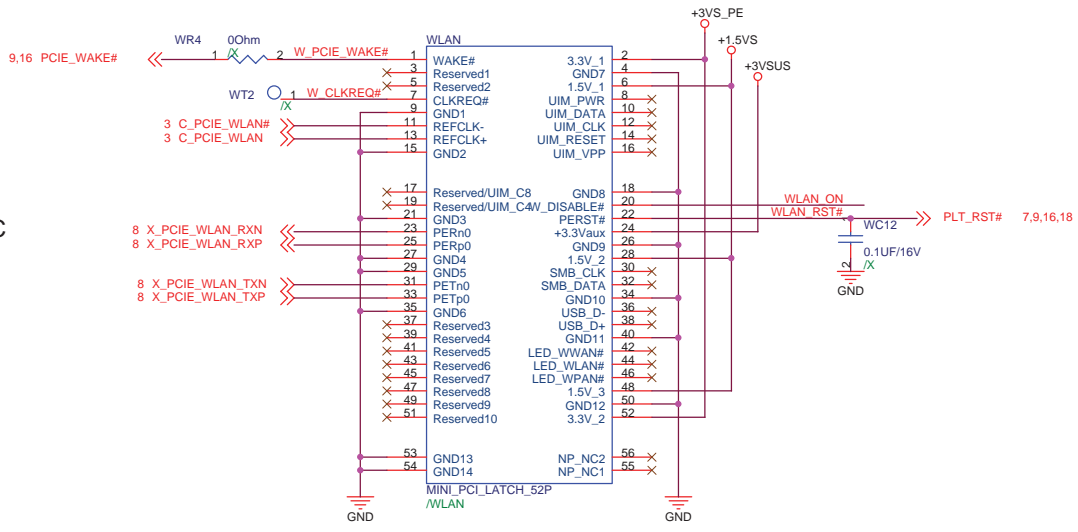
ASUS Title: LAN_AR8132

ASUSTek Computer INC. Engineer: Nicky_Cheng

Size	Project Name	Rev
A3	1015P	1.1G

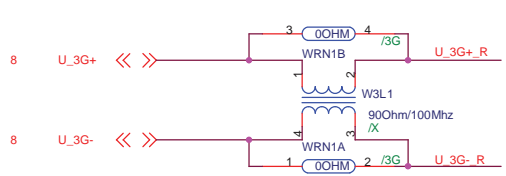
Date: Saturday, February 06, 2010 Sheet 16 of 41

WIFI use PCIE 1.1 Spec
+3VS = 1.0A peak / 0.75A Normal
+1.5VS = 0.5A peak / 0.375A Normal
+3VSUS = 0.375A peak / 0.25A Normal

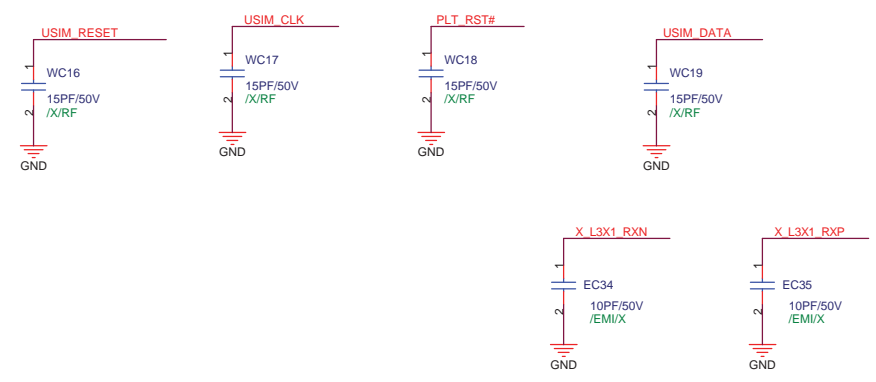
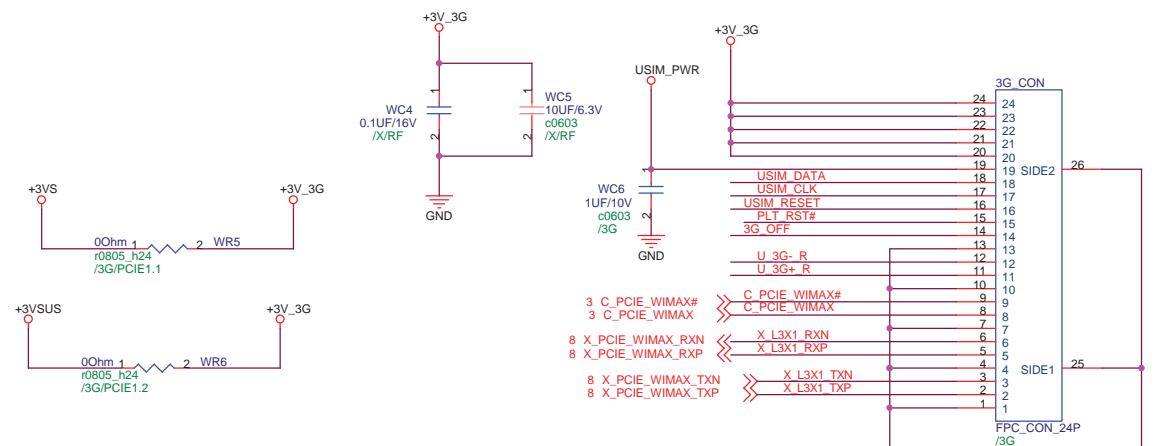
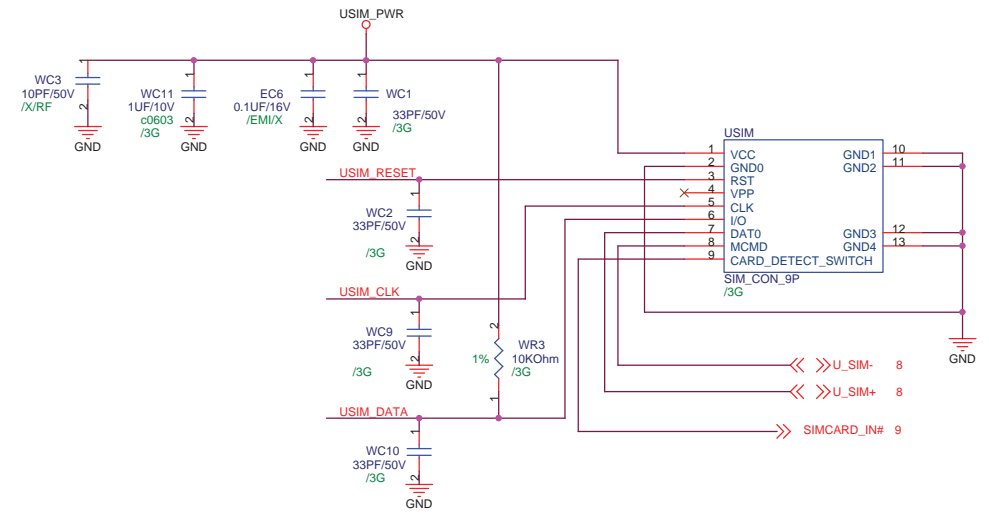


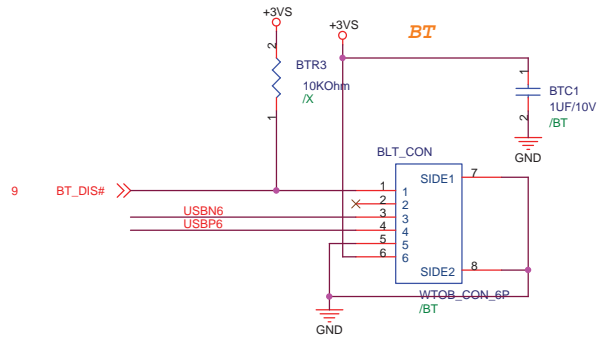
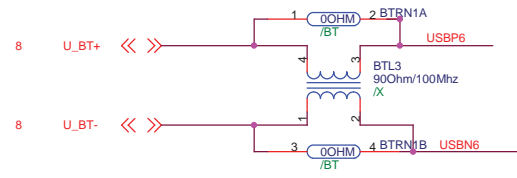
<Core Design>

ASUS		Title : WLAN	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 17 of 42	



7,9,16,17 PLT_RST# >>>
 9 3G_OFF >>>

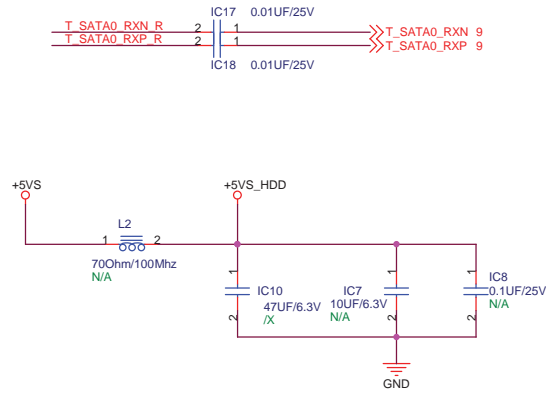
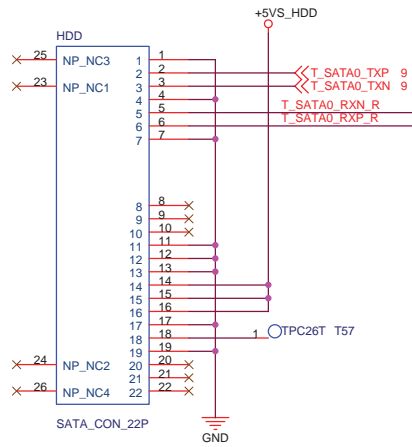




<Core Design>

ASUS		Title : Bluetooth	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size A3	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 19 of 42	

SATA HDD Connector



<Core Design>

ASUS		Title : HD_CON	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size A3	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 20 of 42	

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<Core Design>



Title : USB3.0

ASUSTek Computer INC.


Engineer:

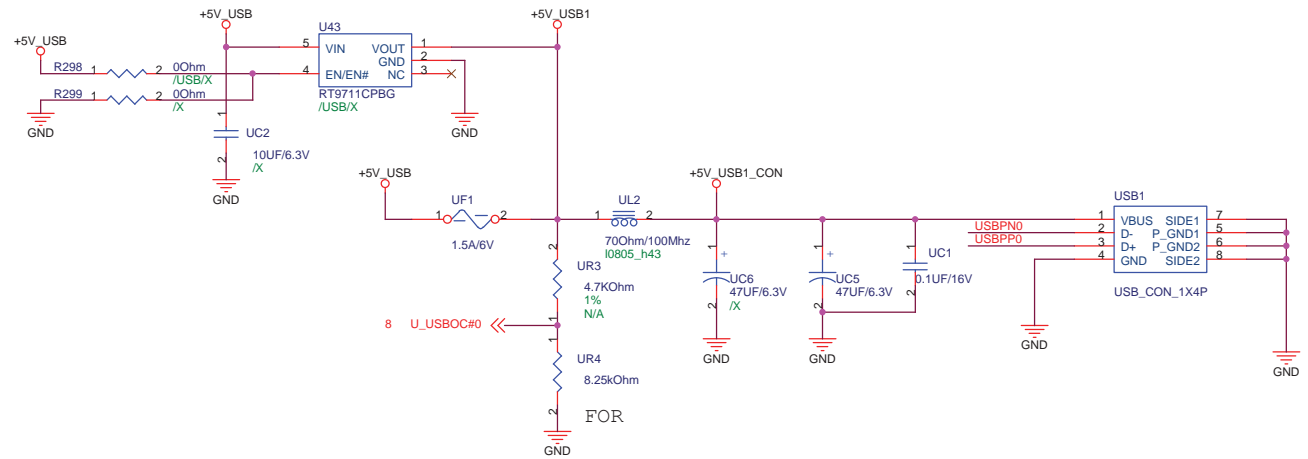
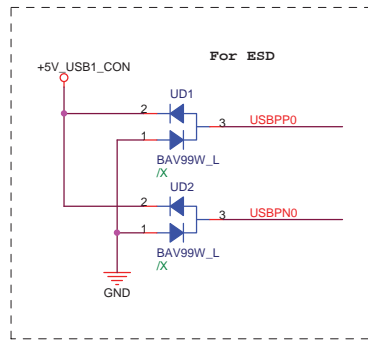
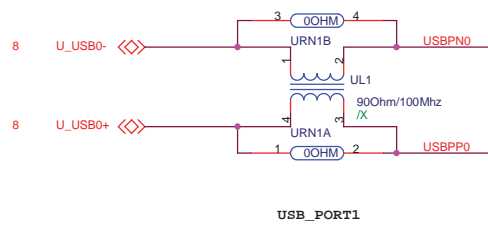
Size	Project Name	Rev
C	1015P	1.1G

Date: Saturday, February 06, 2010 Sheet 21 of 42



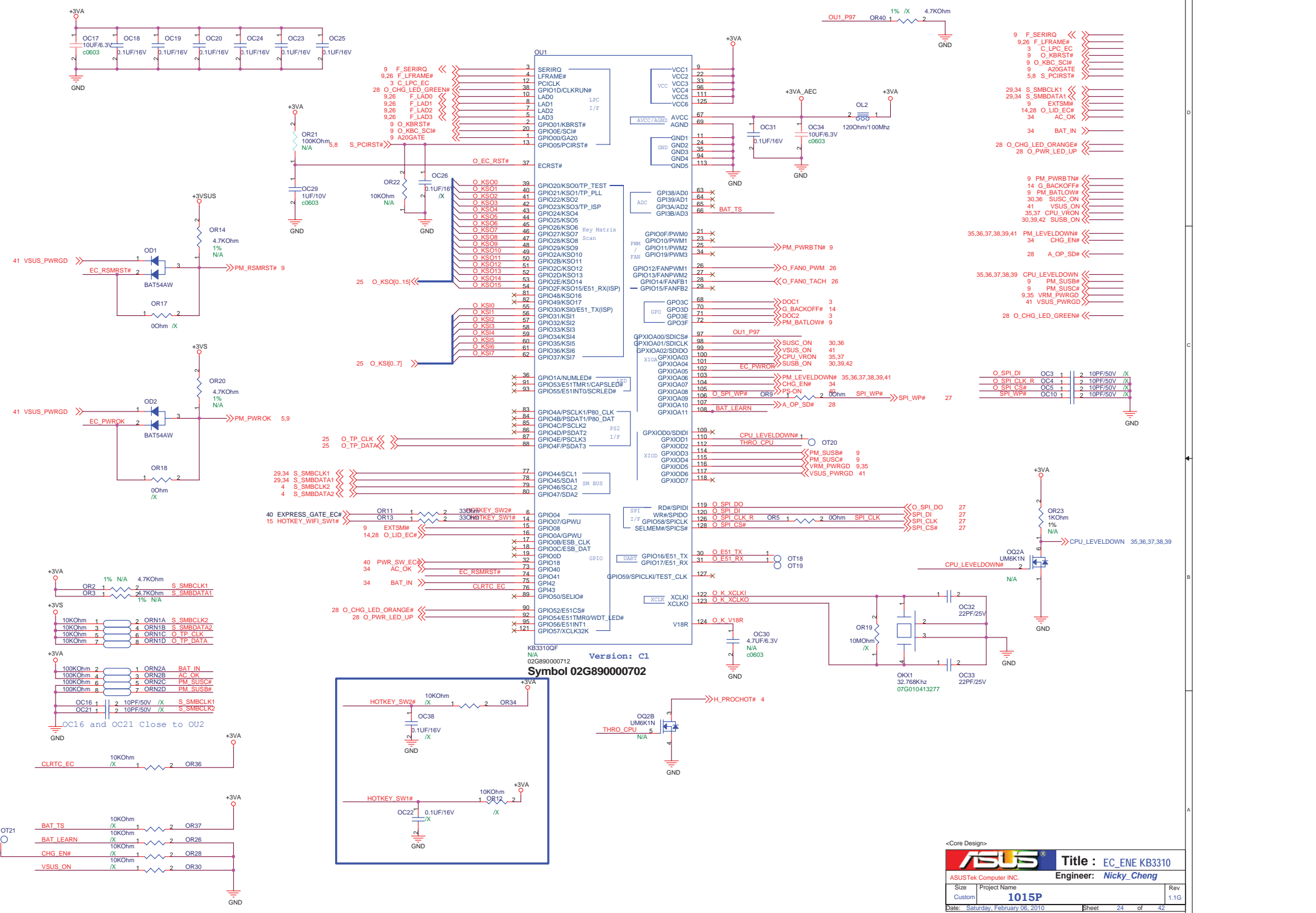
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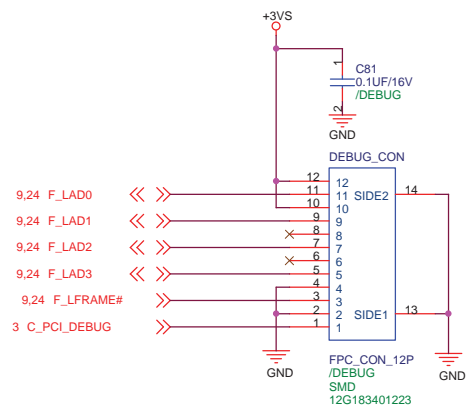
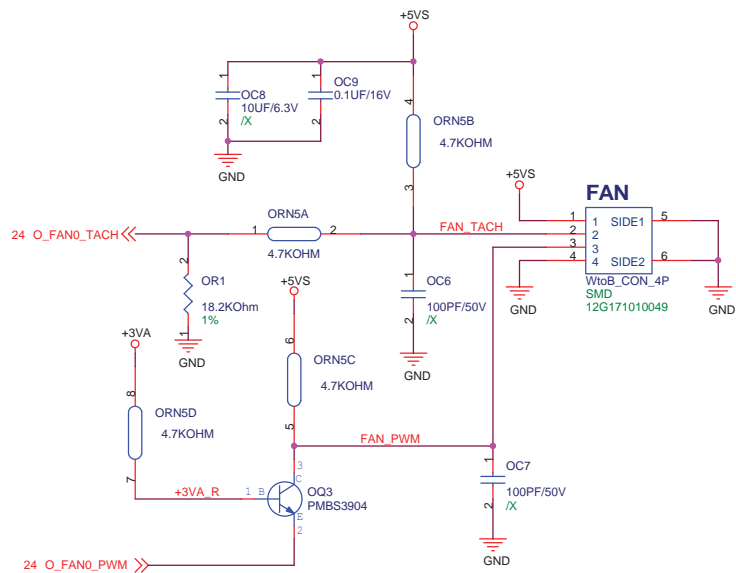
		Title : USB 3.0
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>
Size A3	Project Name 1015P	Rev 1.1G
Date: Saturday, February 06, 2010		Sheet 22 of 42



<Core Design>

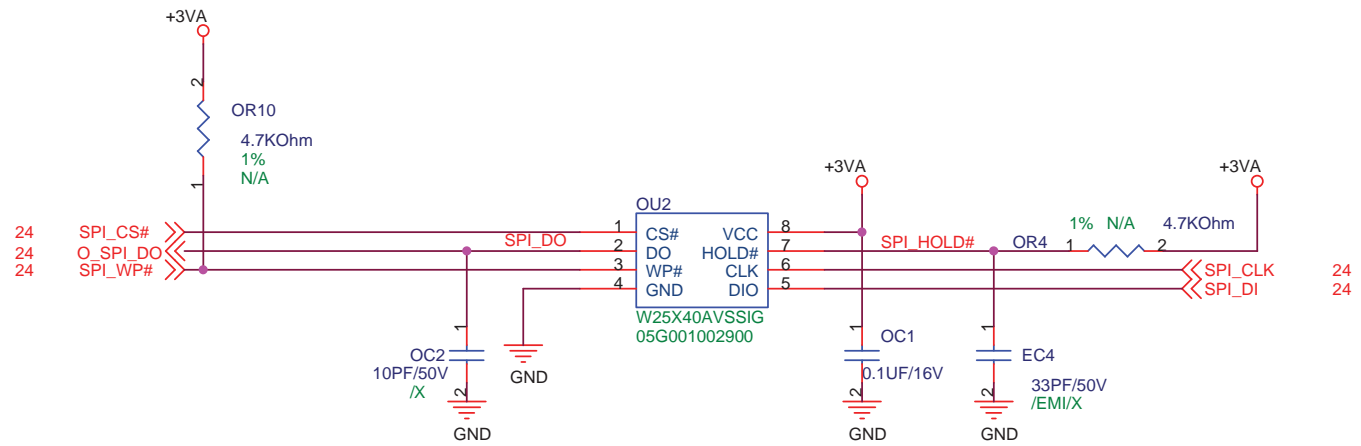
ASUS		Title : USB Port1
ASUSTek Computer INC.		Engineer: Nicky_Cheng
Size	Project Name	Rev
A3	1015P	1.1G
Date: Saturday, February 06, 2010		Sheet 23 of 42





<Core Design>

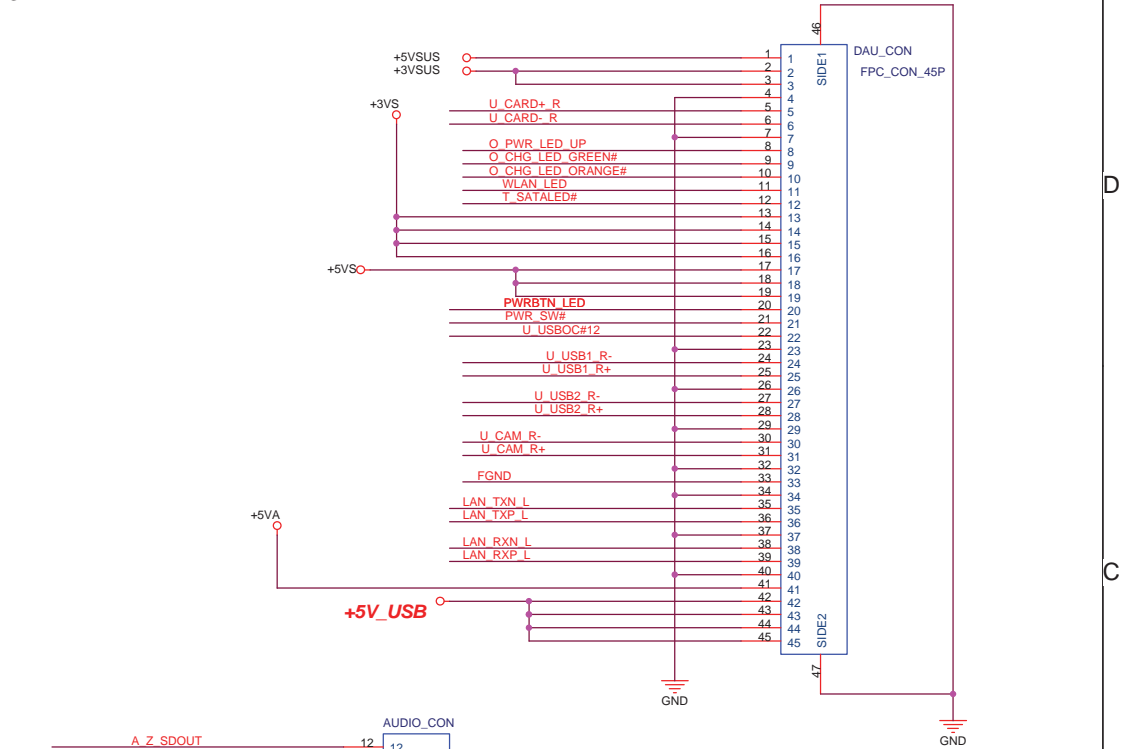
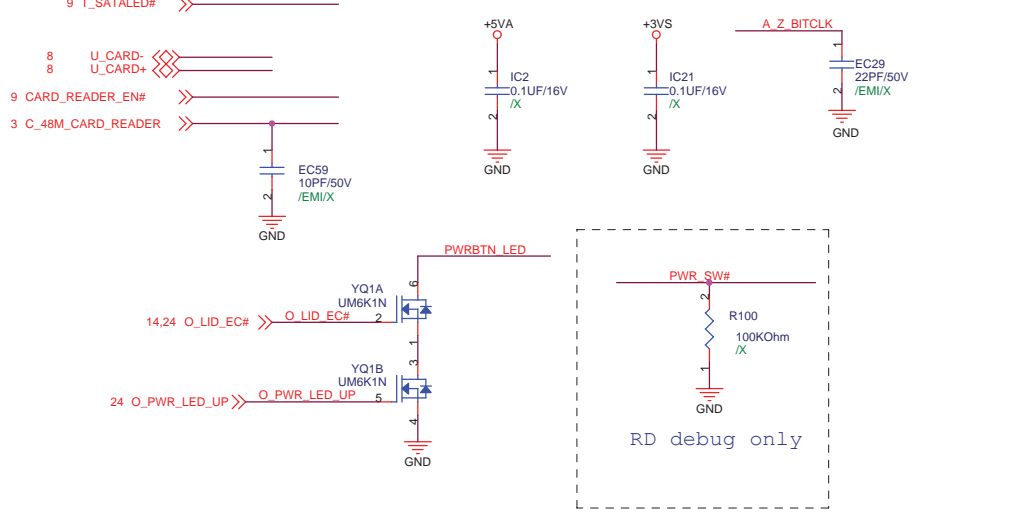
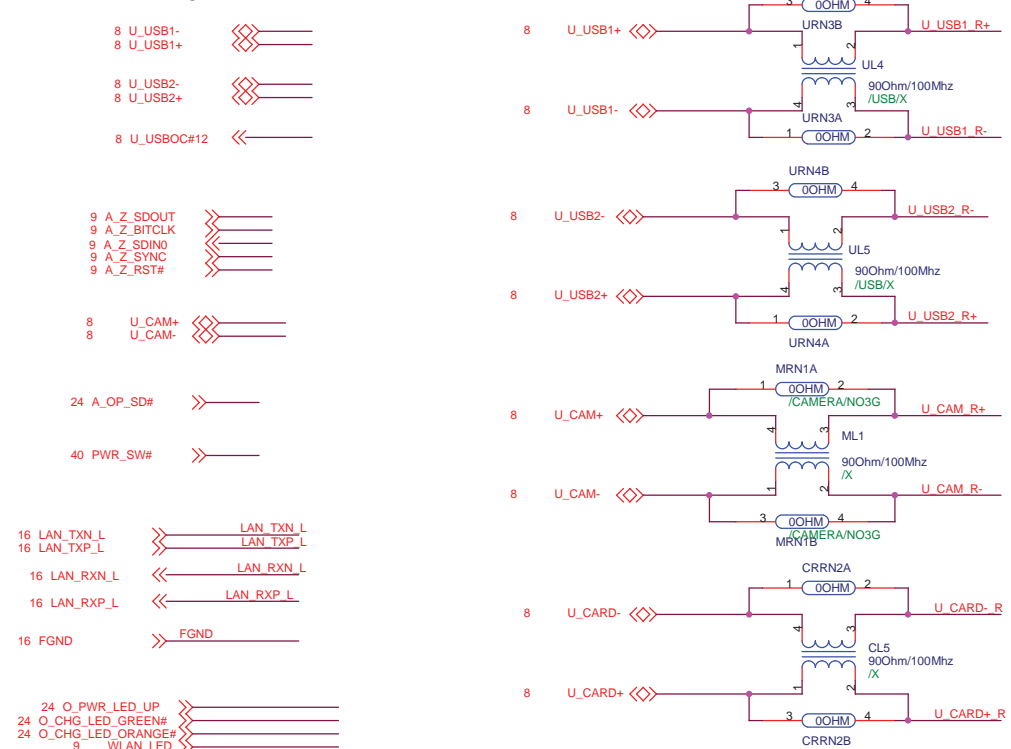
ASUS		Title : Fan_Debug	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size A3	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 26 of 42	



05G001002900;
 05G00100F131;
 05G00100F133

<Core Design>

		Title : SPI_ROM	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A4	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 27 of 42	

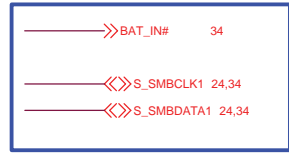


Mode	Adapater Mode	Battery Mode
Scenario	Adapater Mode	Battery Mode
Battery power is between 100%~40%	Orange ON	Green ON
Battery power is between 40%~10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	Green Blinking Quickly
S3/S5 Mode	Scenario the same as above	OFF

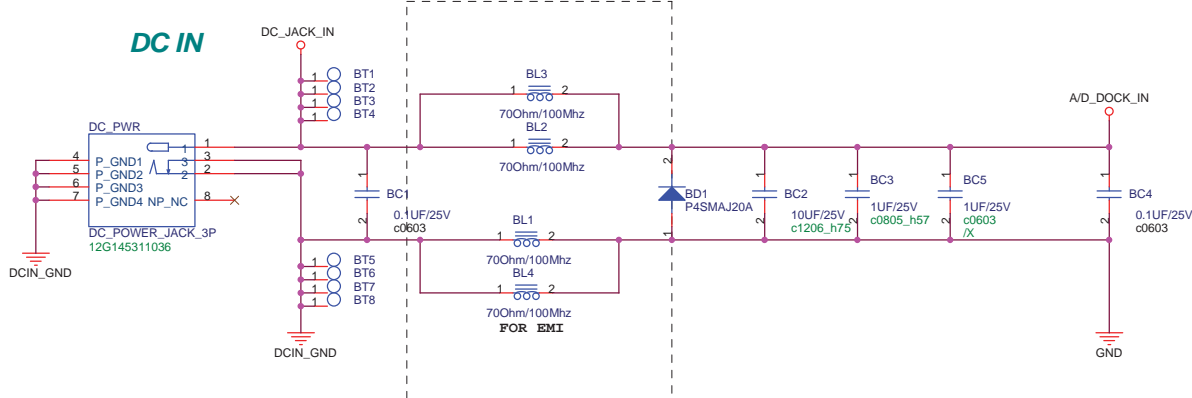
<Core Design>

Title : DUA_CON
ASUS **Engineer:** Nicky_Cheng
 ASUSTek Computer INC.
 Size: A3 Project Name: 1015P Rev: 1.1G
 Date: Saturday, February 06, 2010 Sheet 28 of 42

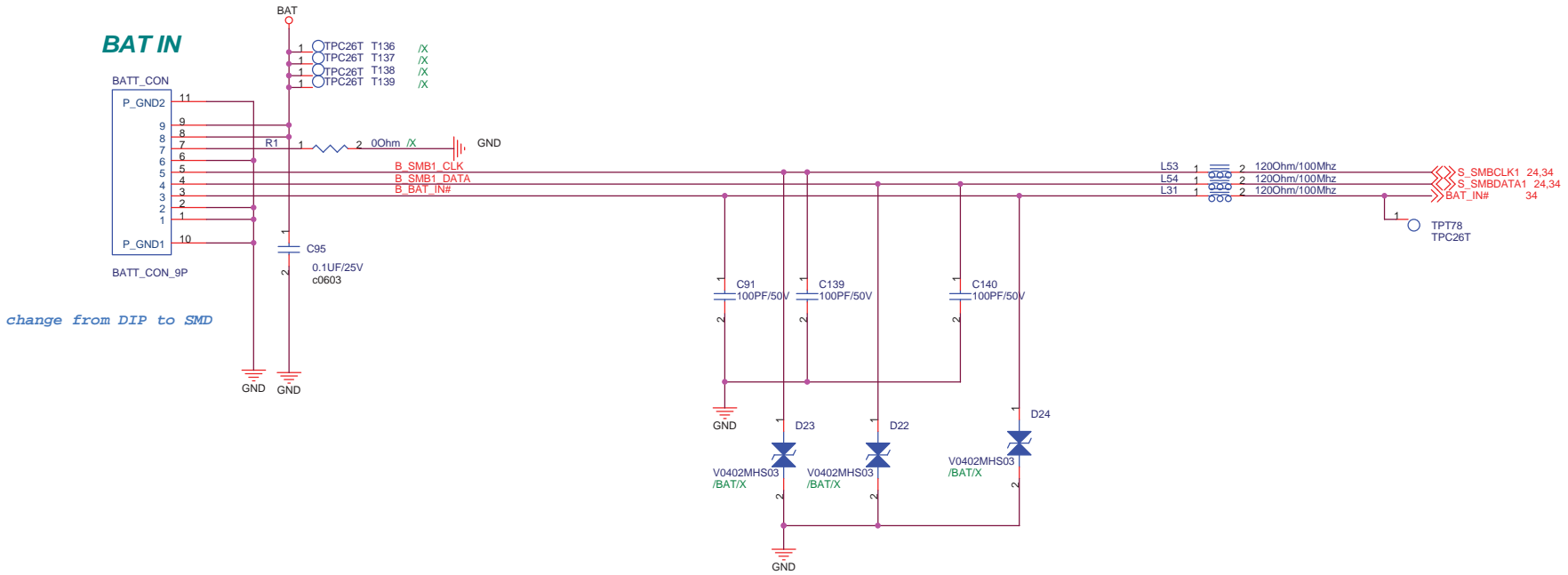
0.1B Beta



DC IN



BAT IN



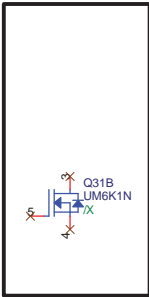
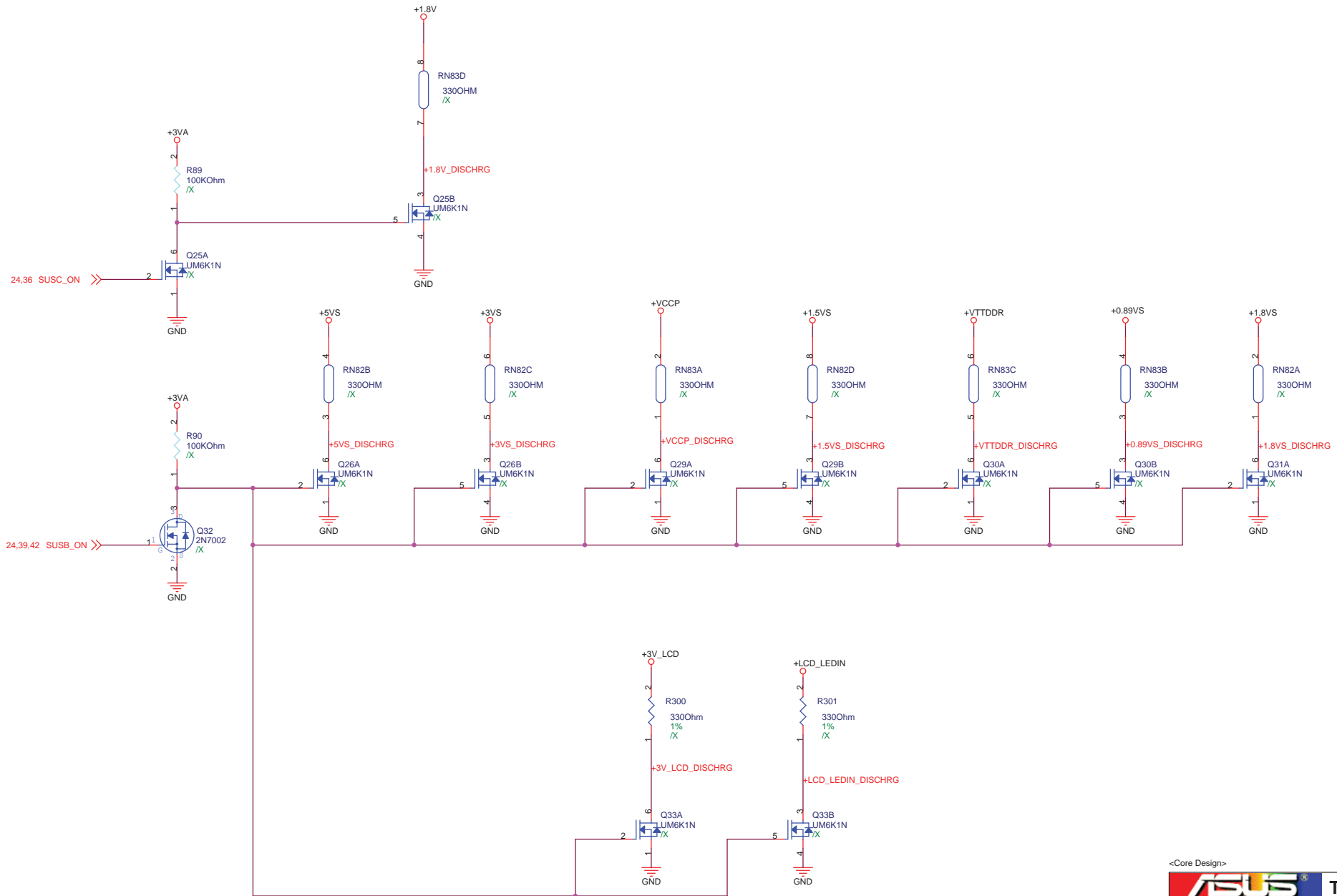
change from DIP to SMD

<Core Design>

ASUS Title : PWR Jack
 ASUSTek Computer INC. Engineer: Nicky_Cheng

Size	Project Name	Rev
A3	1015P	1.1G

Date: Saturday, February 06, 2010 Sheet 29 of 42




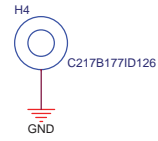
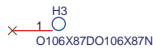
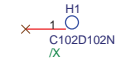
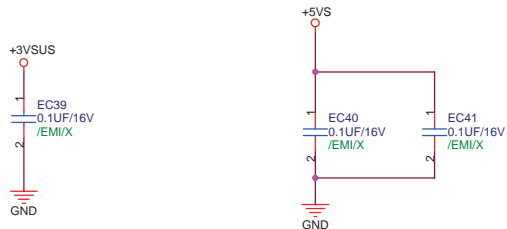
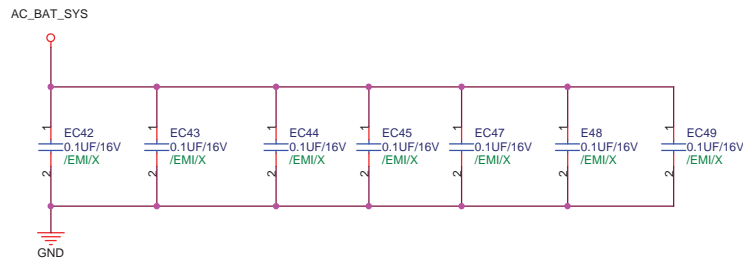
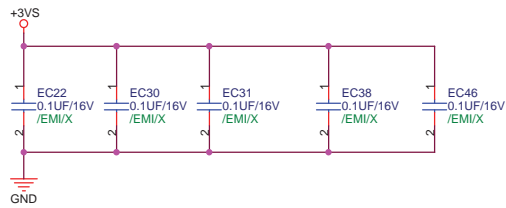
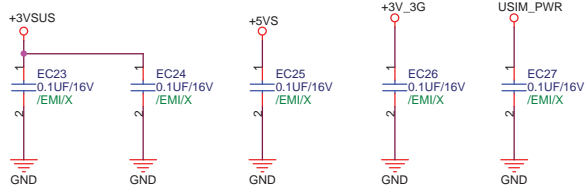
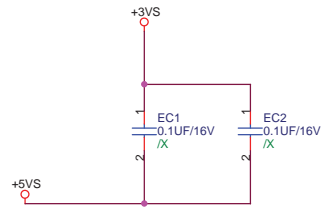
<Core Design>

ASUS		Title : Discharge	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet	30 of 42

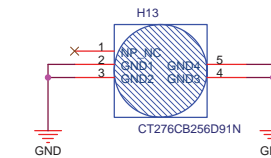
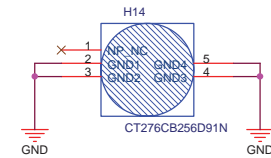
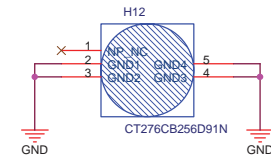
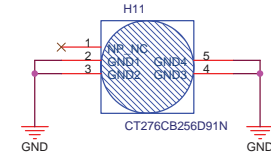
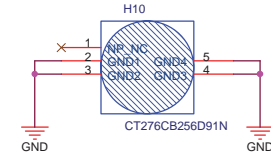
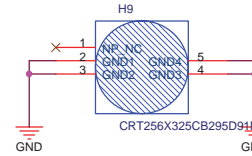
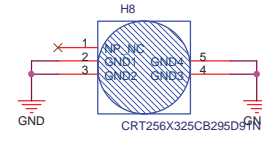
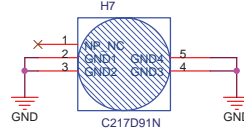
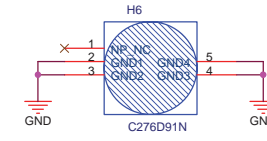
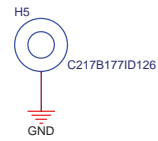


<Core Design>

		Title : SD_CON	
ASUSTek Computer INC.		Engineer: <i>Nicky Cheng</i>	
Size	Project Name		Rev
A3	1015P		1.1G
Date: Saturday, February 06, 2010		Sheet	31 of 42

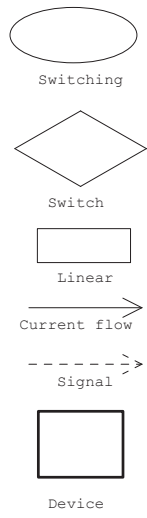
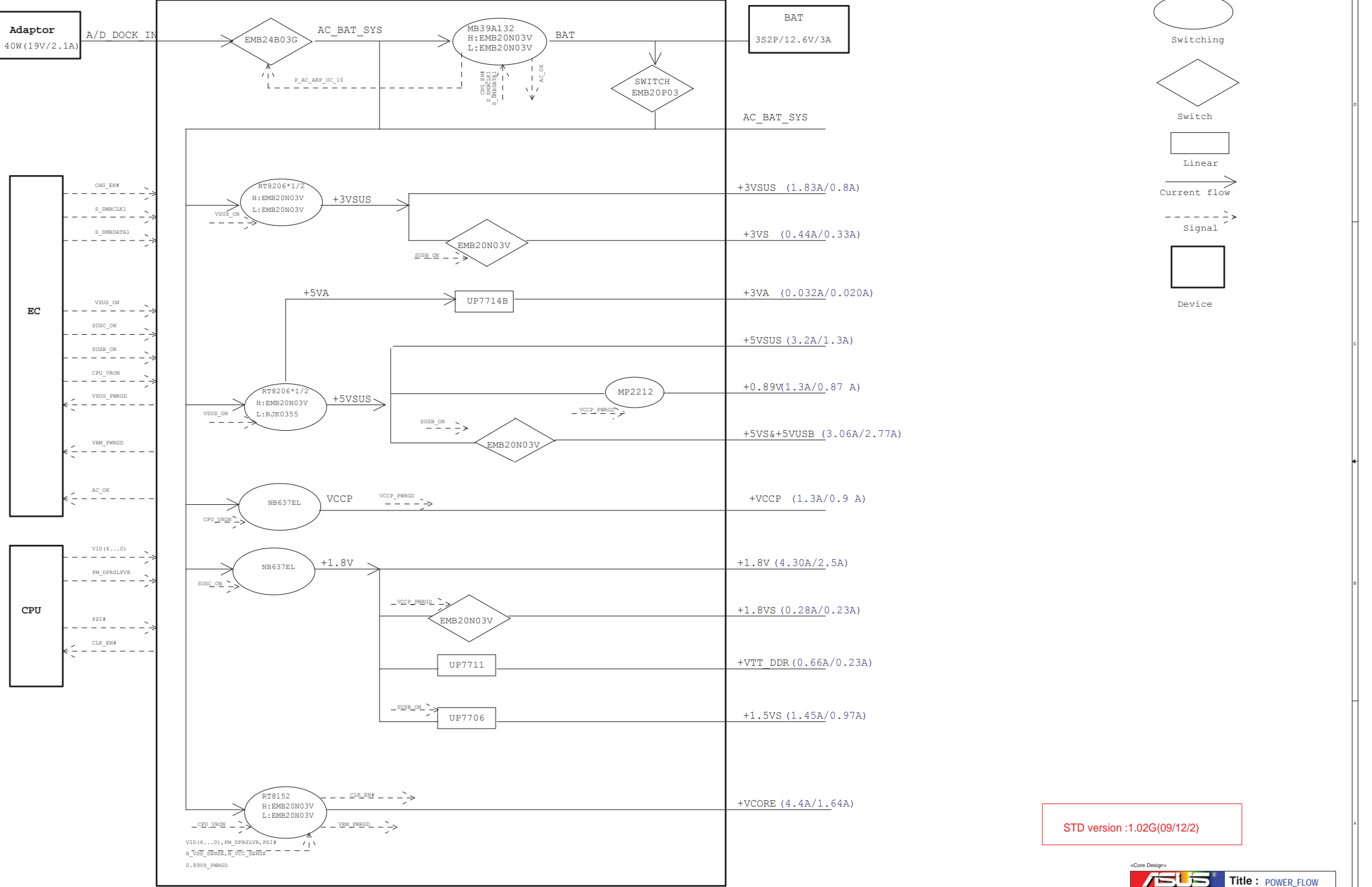


CPU Thermal HOLD

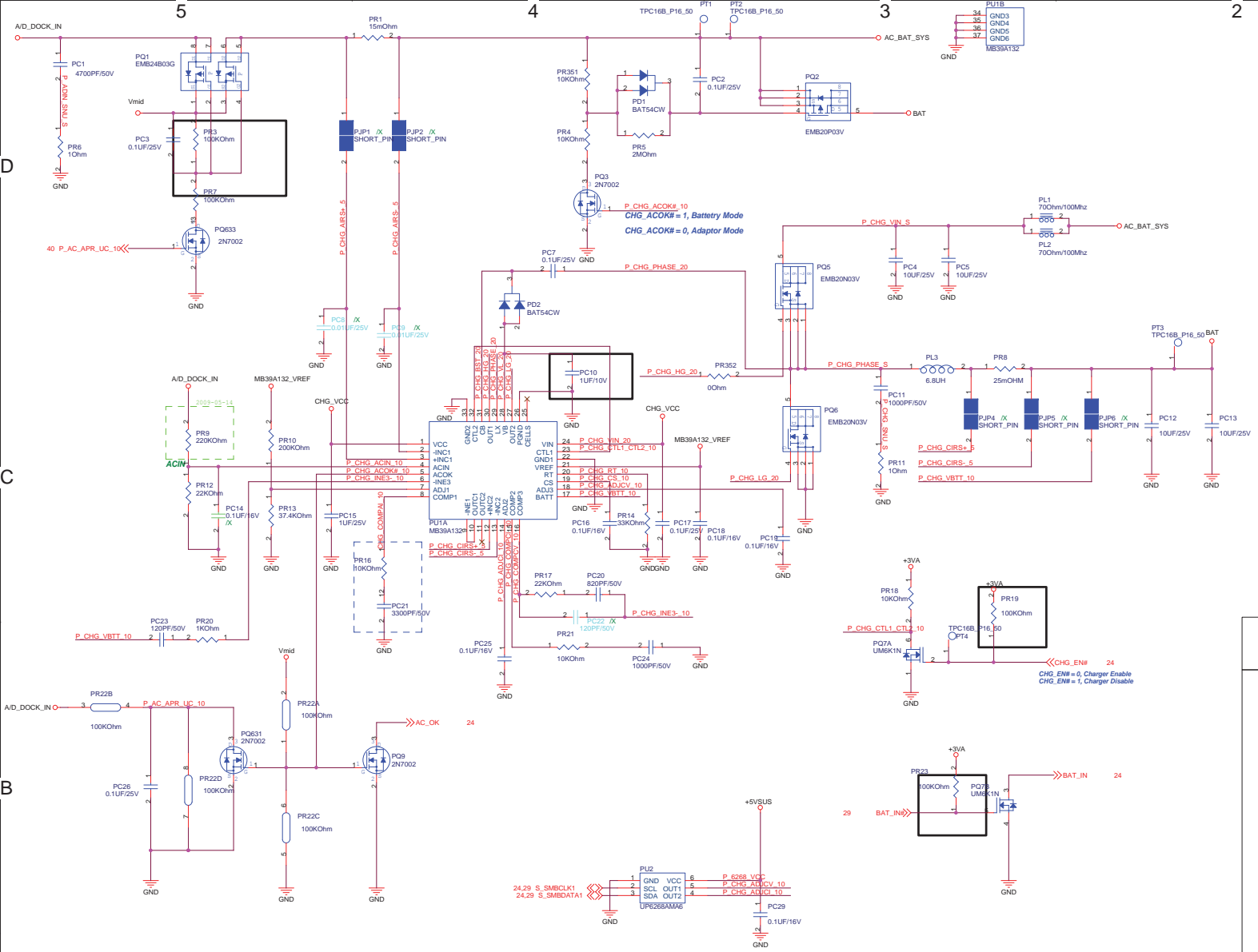


<Core Design>

ASUS		Title : SREW HOLE&EMI	
ASUSTek Computer INC.		Engineer: <i>Nicky_Cheng</i>	
Size	Project Name	Rev	
A3	1015P	1.1G	
Date: Saturday, February 06, 2010		Sheet	32 of 42



STD version : 1.02G(09/12/2)

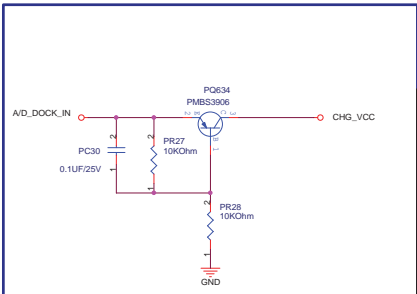


Power stage

- I/P Current:**
 $I_{in} = V_o * I_o / (0.8 * V_{in}) = 1.64A$
- Ripple Current:**
 $I_{rip} = 1.18A$
 $I_{spec} = 2A$
 $\phi 1 pcs$
- Inductor Spec:**
 $I_{sat} = 10A$
 $I_{dc} = 5.5A$
 $DCR = 37m\Omega$
- MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\leq 10\mu s$)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\leq 10\mu s$)

Controller

- Voltage & Current:**
+12.6V @ 2.5A
- Frequency:**
PR122=33KOHM,
Fosc=515KHz
- OCp:**
- POR:**
POR Hysteresis = 0.1V
V on = 7.5V
- Enable Voltage:**
V = 2.9V
- Soft start time:**
Tss=23ms
- Phase selection:**
N/A
- Inrush Current:**
C total = 20uF
I inrush = 0.01A

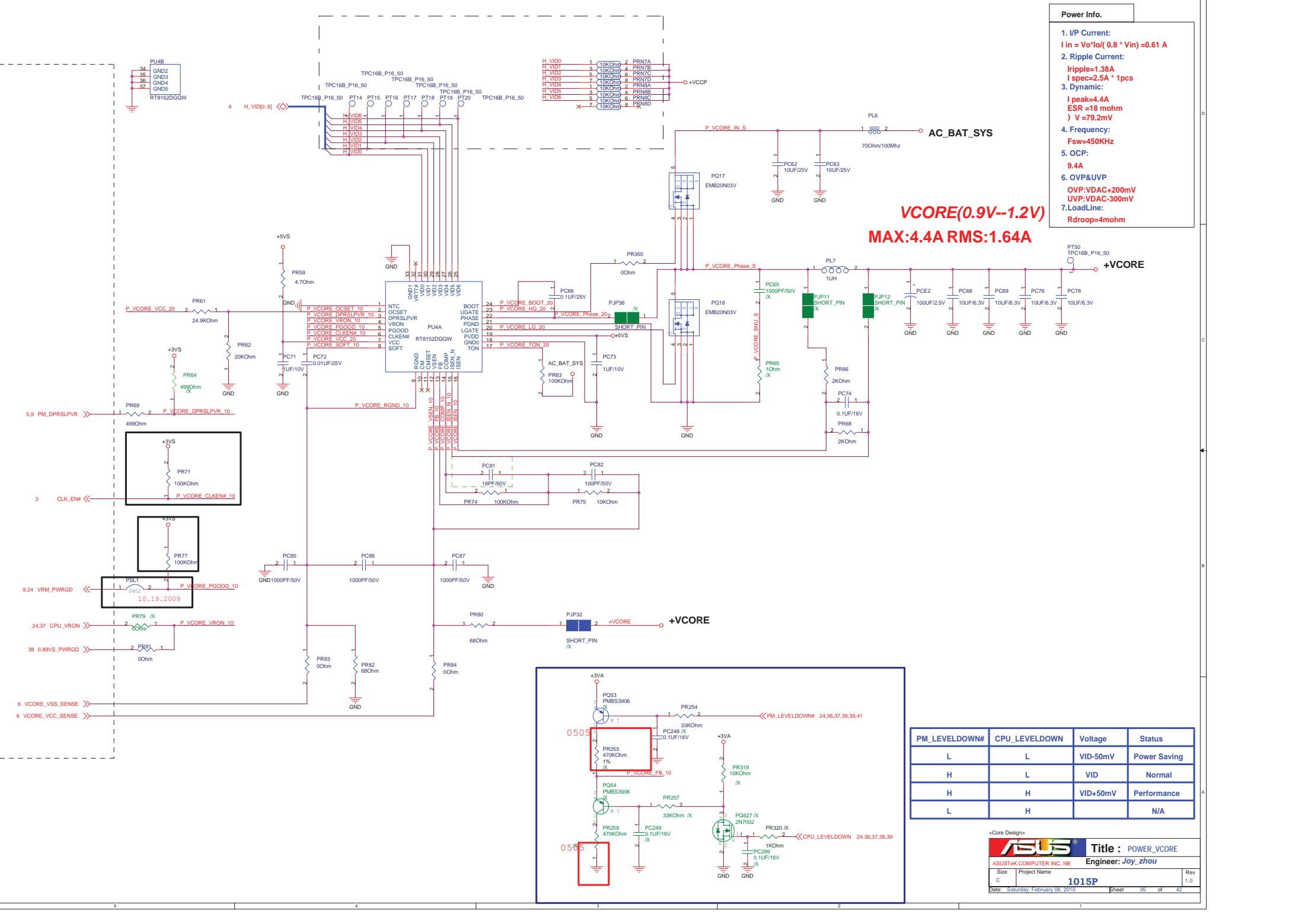


Battery Charging Current :
 $4.4V > V_{adj2} \geq 0V \implies$
 $I_{chg} = (V_{adj2} - 0.075) / (25 * R_s)$
 BATSEL_2P# = 1, $I_{ch} = 1.49A$
 BATSEL_2P# = 0, $I_{ch} = 2.62A$
Input Adaptor Max. Current Limit :
 $I_{limit_current} = (V_{adj1} - 0.075) / (25 * R_s) = 1.90A$

Pre-Charging Mode :
 Precharging current = 149.2mA
 $V_{adj2} = 168mV$
ACIN Threshold = 1.25V
 Adaptor > 13.75V, System Powered by Adaptor
 Adaptor < 13.75V, System Powered by Battery

Battery Charging Voltage :
 $V_{adj3} : V_{REF} \implies V_{bat} = 4.2V / cell$
 $3.9V > V_{adj3} > 2.4V \implies V_{bat} = 4.35V / cell$
 $V_{adj3} : GND \implies V_{bat} = 4.0V / cell$
 $2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 * V_{adj3}$
Battery Cell Selection :
 CELLS: VREF $\implies 4$ Cells;
 CELLS: OPEN $\implies 3$ Cells;
 CELLS: GND $\implies 2$ Cells;

VREF = 5.0V
 $f_{osc}(KHz) = 17000 / RT (K\Omega)$
 Soft start: $ts(s) = 0.13 * CS (\mu F)$

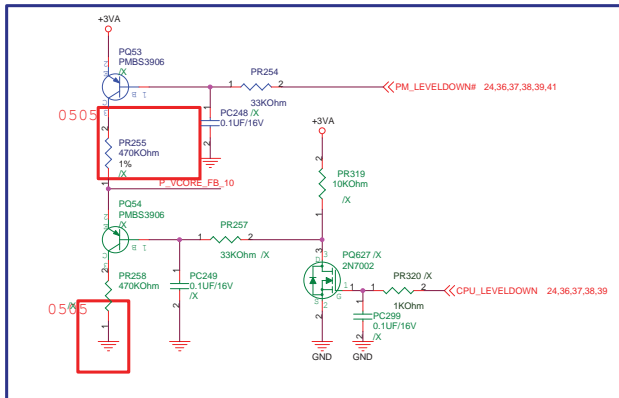


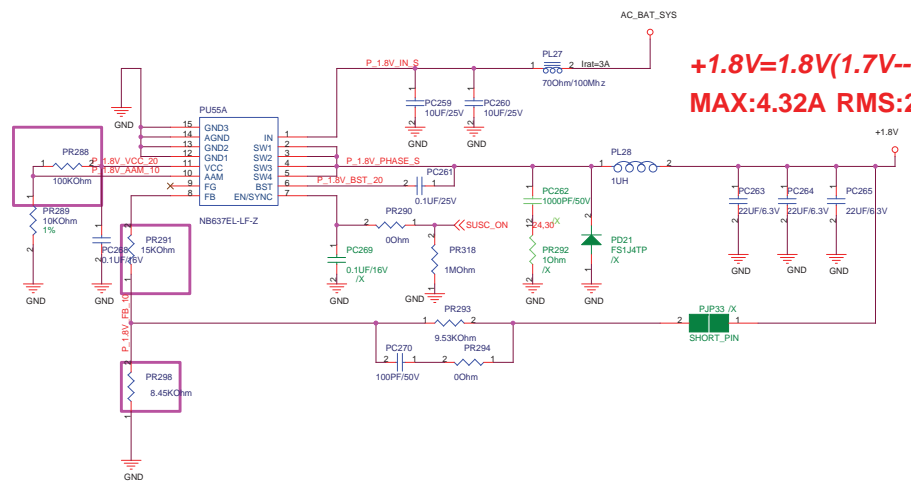
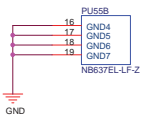
Power Info.

- I/P Current:
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.61 \text{ A}$
- Ripple Current:
 $I_{ripple} = 1.38 \text{ A}$
 $I_{spec} = 2.5 \text{ A} \cdot 1 \text{ pcs}$
- Dynamic:
 $I_{peak} = 4.4 \text{ A}$
 $ESR = 18 \text{ mohm}$
 $V = 79.2 \text{ mV}$
- Frequency:
 $F_{sw} = 450 \text{ KHz}$
- OC:
 9.4 A
- OVP&UVP
 $OVP = V_{DAC} + 200 \text{ mV}$
 $UVP = V_{DAC} - 300 \text{ mV}$
- LoadLine:
 $R_{droop} = 4 \text{ mohm}$

**VCORE(0.9V--1.2V)
MAX:4.4A RMS:1.64A**

PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	VID-50mV	Power Saving
H	L	VID	Normal
H	H	VID+50mV	Performance
L	H		N/A





+1.8V=1.8V(1.7V--1.8V)
MAX:4.32A RMS:2.5A

Power Info.

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.08A$
- Ripple Current:**
 $I_{rip} = 1A$
- Frequency:**
 $F_{osc} = 600KHz$
- Current Limit:**
6A

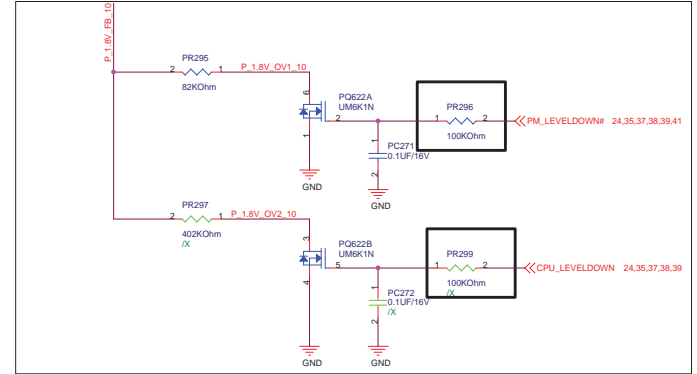
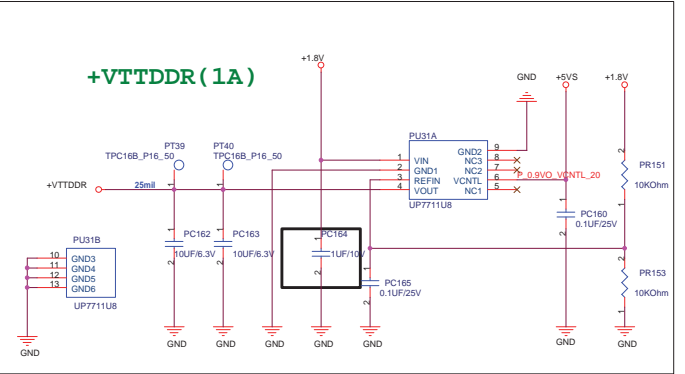
0.9VS@1A

- Dropout Voltage:**
 $V = 0.3V (I_o = 2A)$
- Current Limit:**
 $I_{limit} = 4A$
- Continue Current:**
 $I_{cont} = 3A$
- Power Dissipation:**
 $R_{thjc} = 52 /W$
 $P_d = 1.9W$

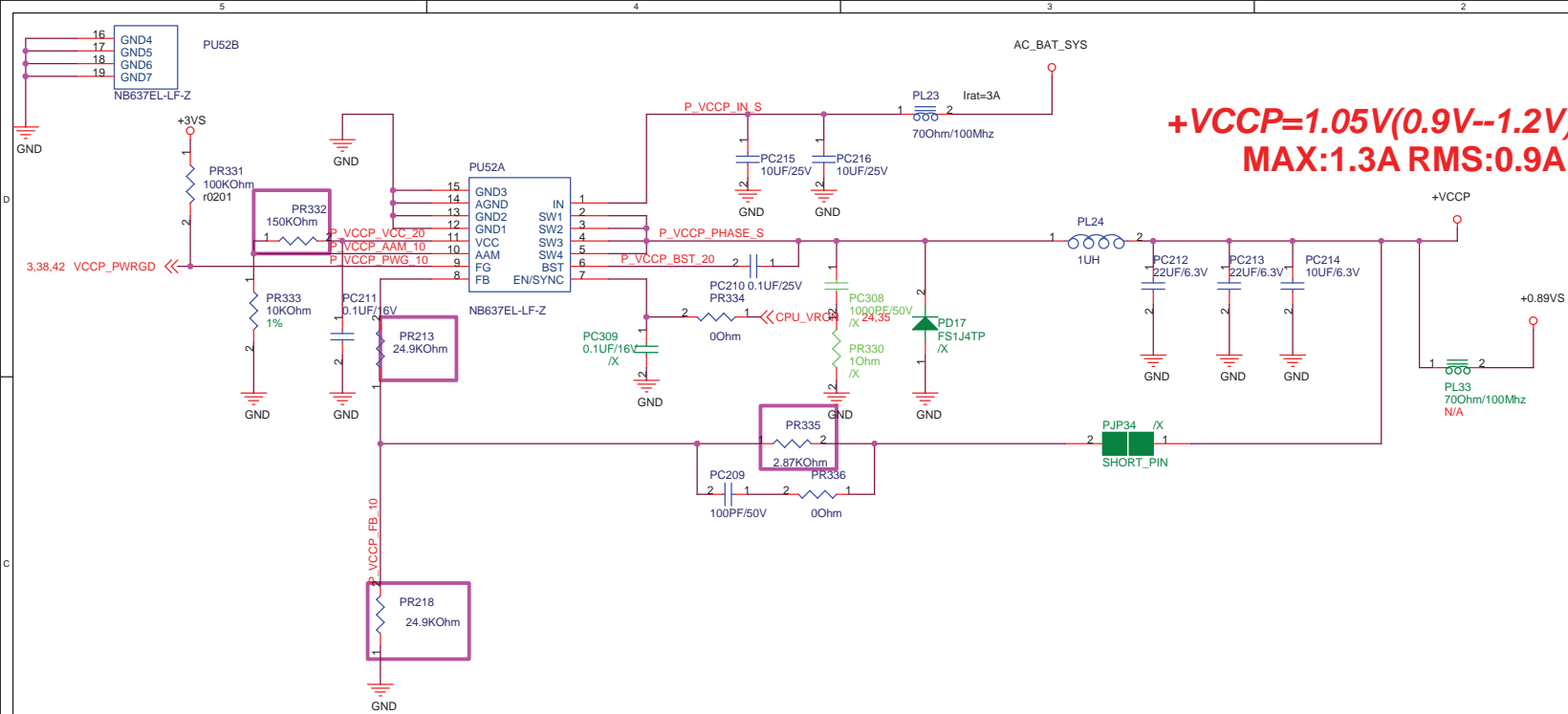


PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.670V	Power Saving
H	L	H	1.800V	Normal
H	H	L	1.912V	Performance
L	H	L		

+VTTDDR (1A)

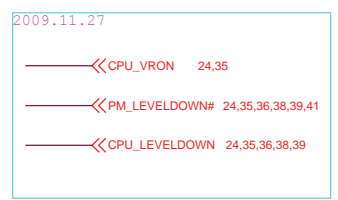


ASUS
 ASUSTek Computer INC
 Title: +1.8V&VTTDDR
 Engineer: Joy_Zhou
 Project Name: 101SP
 Date: Saturday, February 08, 2010
 Sheet: 36 of 42

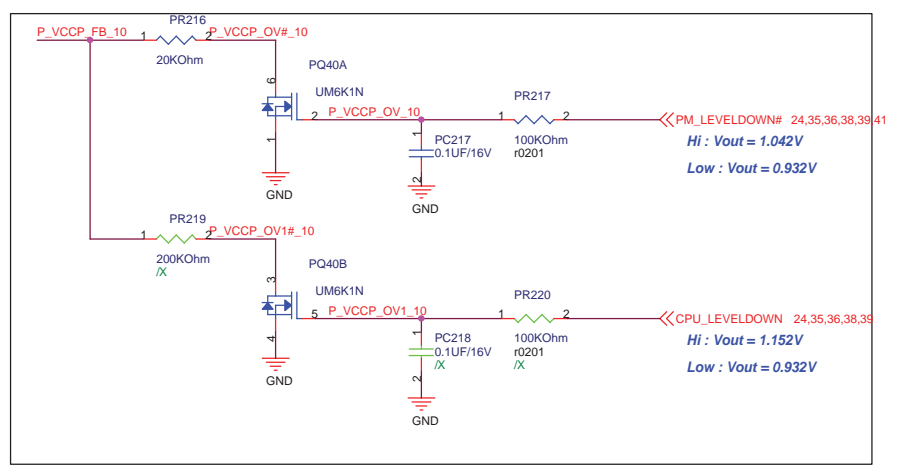


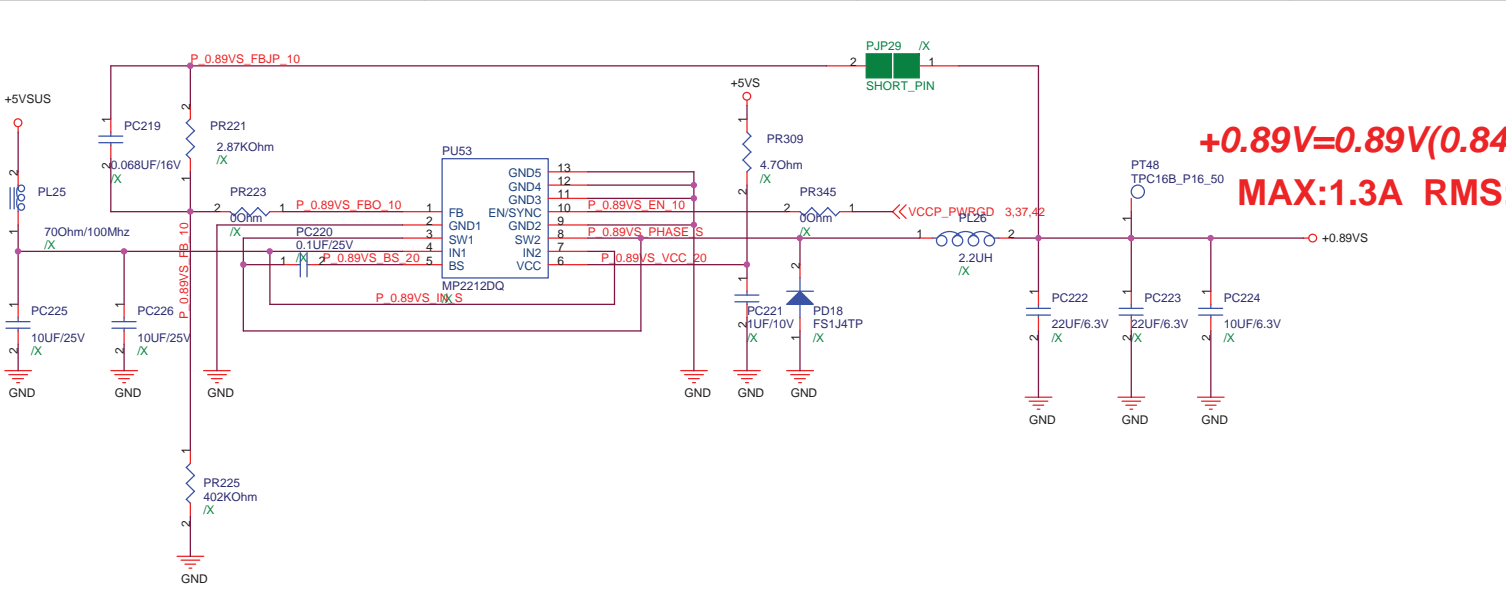
Power Info.

1. I/P Current:
 $I_{in} = V_o * I_o / (0.8 * V_{in}) = 0.7A$
2. Ripple Current:
 $I_{rip} = 1.08A$
 $I_{spec} = 2.5A \odot 1$
3. Frequency:
 $F_{osc} = 600KHz$
4. Current Limit:
6A



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.932V	Power Saving
H	L	H	1.042V	Normal
H	H	L	1.127V	Performance
L	H	L		N/A

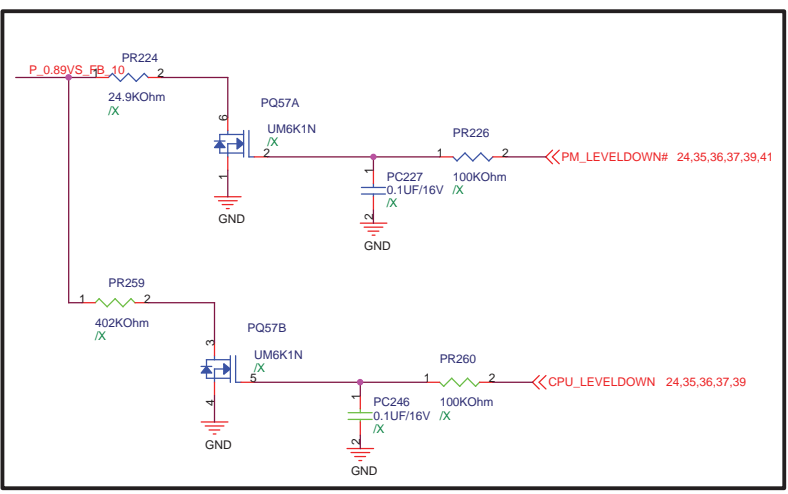
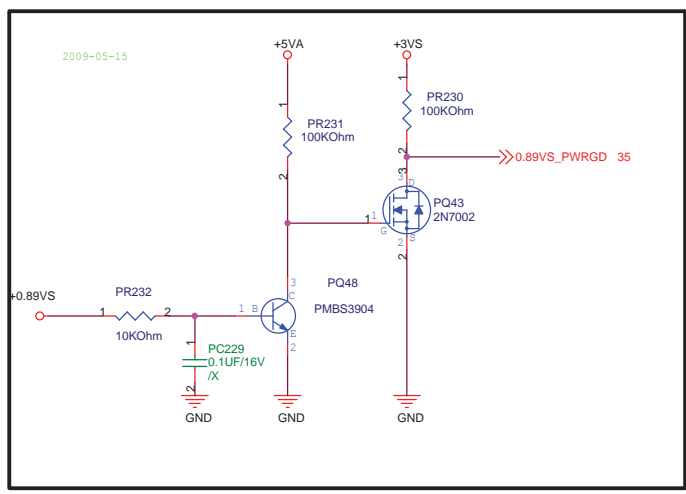
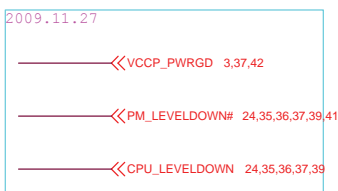




+0.89V=0.89V(0.844V--0.95V)
MAX:1.3A RMS:0.87A

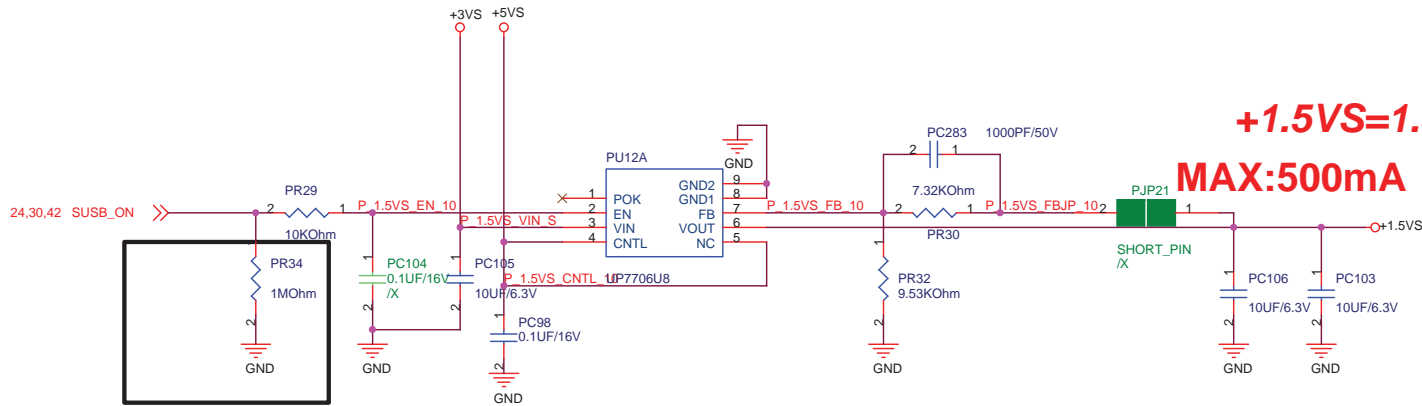
Power Info.

- I/P Current:**
 $I_{in} = V_o * I_o / (0.8 * V_{in}) = 0.36A$
- Ripple Current:**
 $I_{rip} = 0.61A$
 $I_{spec} = 2.5A * 1pcs$
- Dynamic:**
 $I_{peak} = 1.6A$
 $ESR = 18\text{ mohm}$
 $V = 28.8mV$
- Frequency:**
 $F_{osc} = 600KHz$
- Current Limit:**
6A



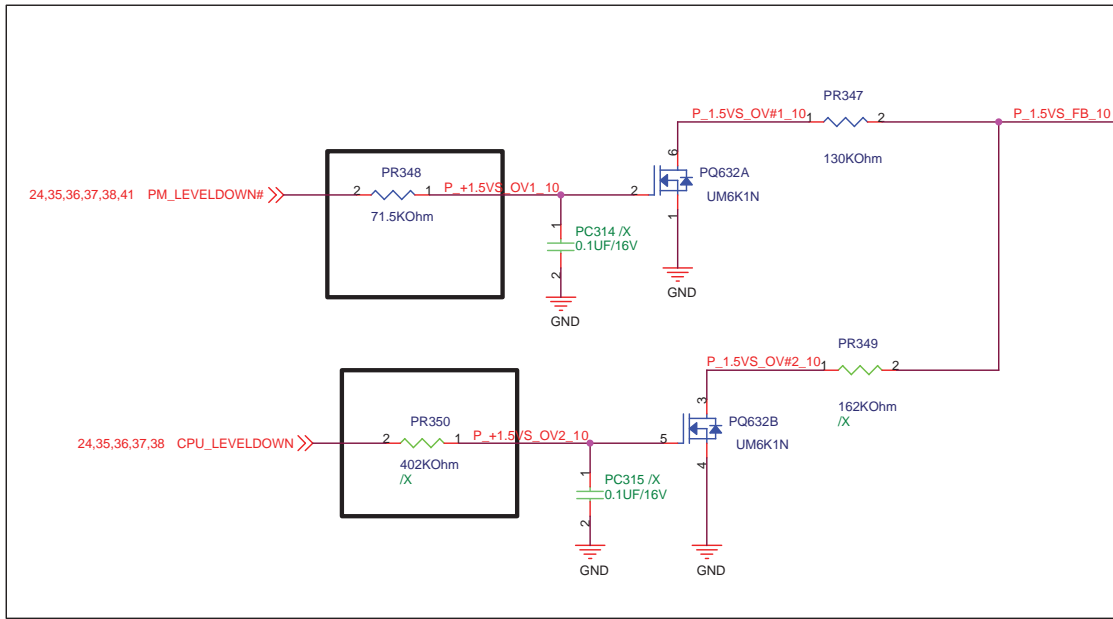
PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	0.844V	Power Saving
H	L	0.897V	Normal
H	H	0.950V	Performance
L	H		N/A

<Core Design>
ASUS Title : +1.5VS & +2.5VS
 ASUSTek Computer INC Engineer: Joy_Zhou
 Size Project Name Rev
 A3 1015P 1.0
 Date: Saturday, February 06, 2010 Sheet 38 of 42

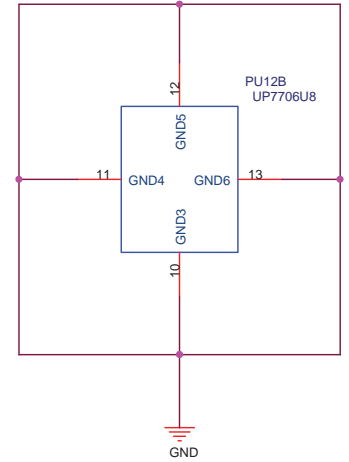


+1.5VS=1.5V(1.44V--1.5V)
MAX:500mA RMS:350mA

- 1. Dropout Voltage:
 $V = 300\text{ mV}$ ($I_o = 2A$)
- 2. Current Limit:
 $I_{\text{limit}} = 2.8A$
- 3. Pd:
 $R_{\text{thjc}} = 5\text{ C/W}$
 $P_d = 1.9W$



2009.11.27
 24,30,42 SUSB_ON >>
 24,35,36,37,38,41 PM_LEVELDOWN# >>
 24,35,36,37,38 CPU_LEVELDOWN# >>



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	1.41V	Power Saving
H	L	1.49V	Normal
H	H	1.51V	Performance
L	H	1.50V	

<Core Design>

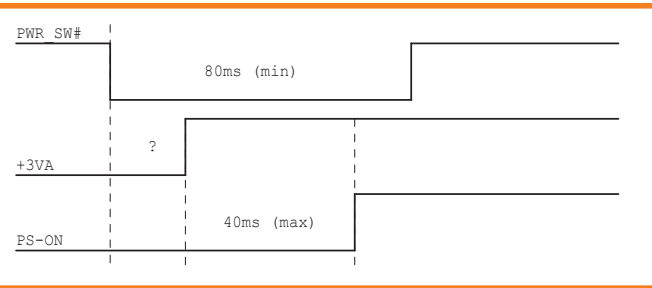
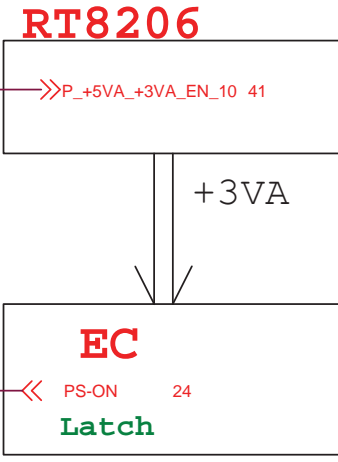
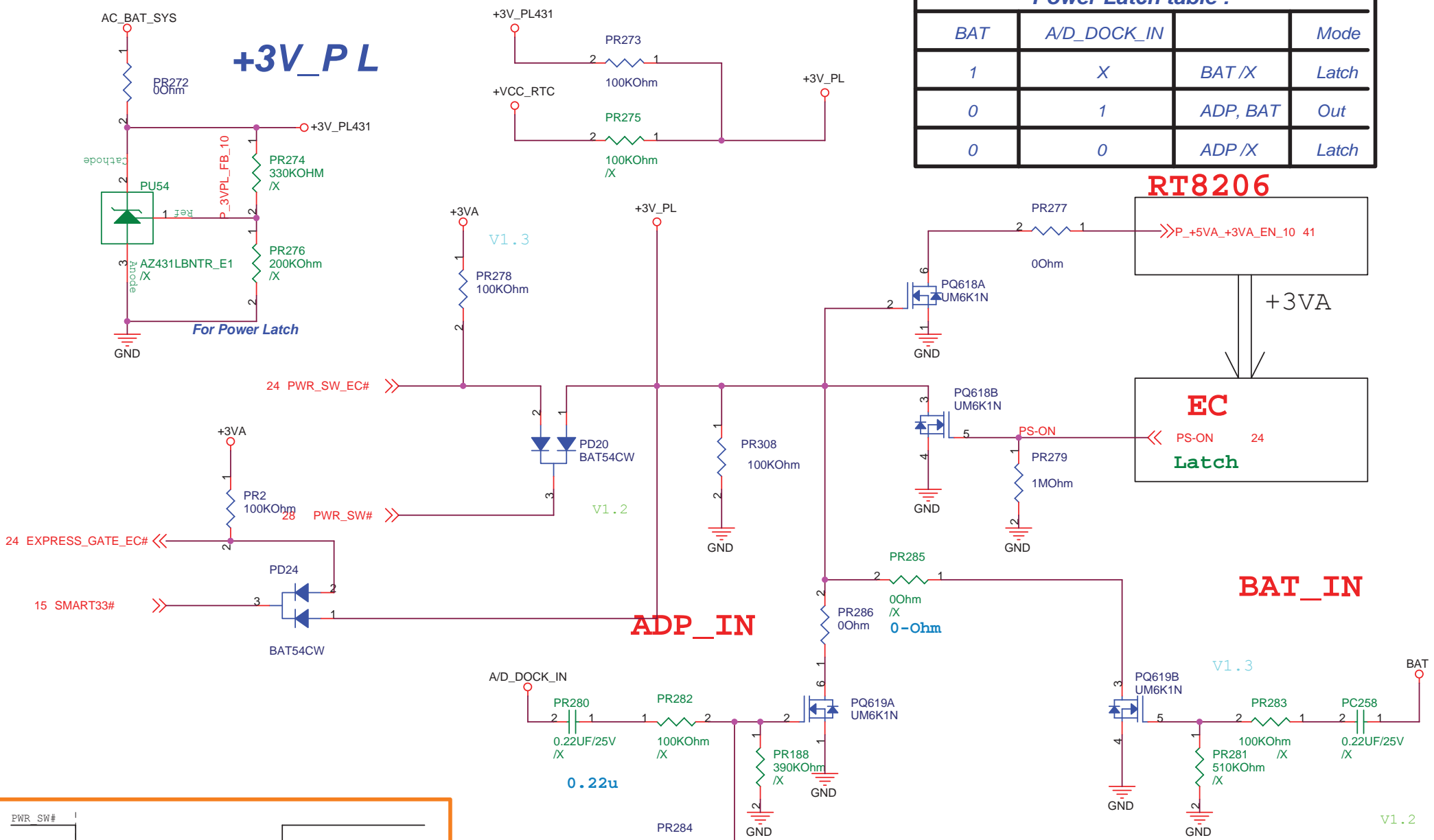
ASUS Title : +1.5VS & +2.5VS
 ASUSTek Computer INC Engineer: Joy_Zhou

Size	Project Name	Rev
B	1015P	1.0

Date: Saturday, February 06, 2010 Sheet 39 of 42

Power Latch table :

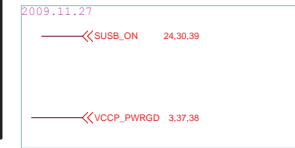
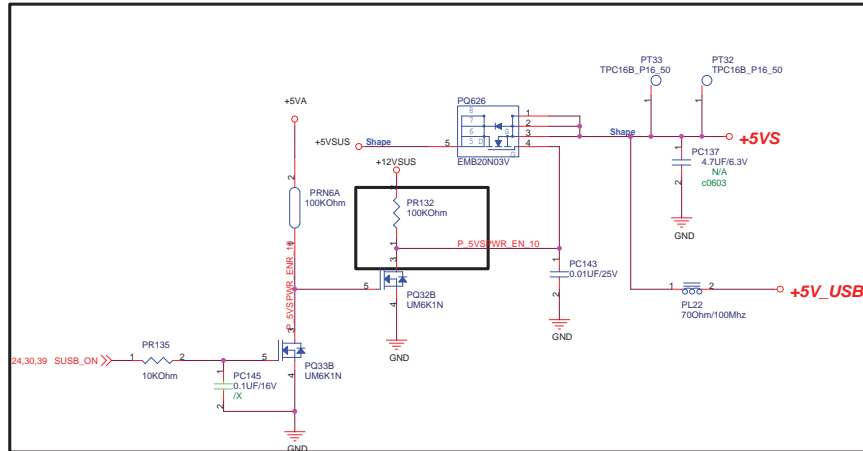
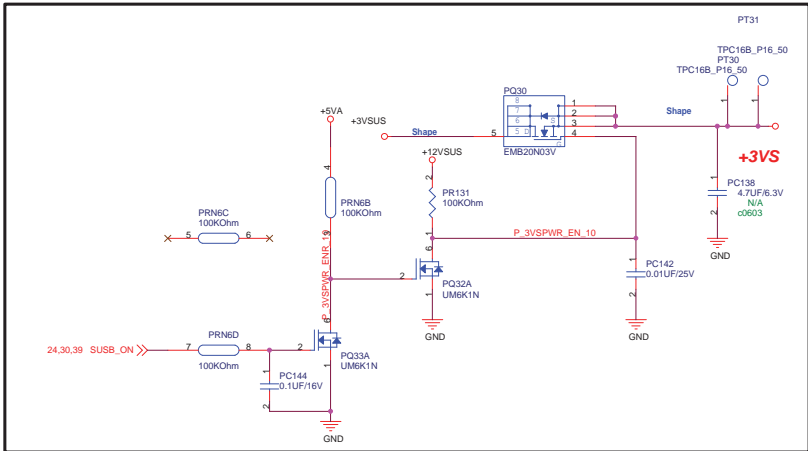
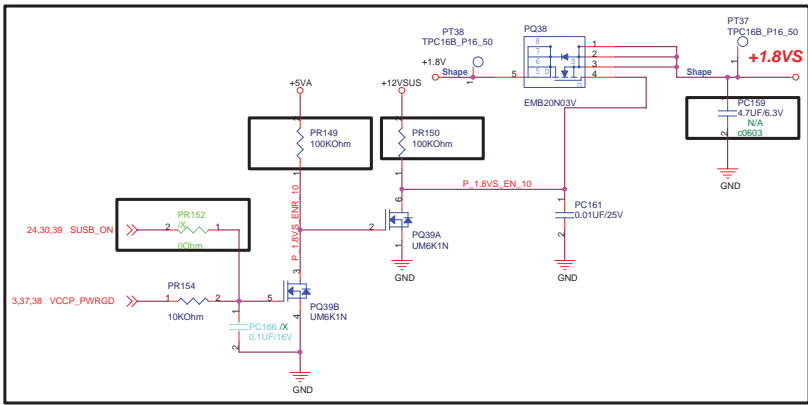
BAT	A/D_DOCK_IN		Mode
1	X	BAT /X	Latch
0	1	ADP, BAT	Out
0	0	ADP /X	Latch



V1.2 For ADP power latch

<Core Design>

ASUS		Title : Power Latch	
ASUSTek Computer INC.		Engineer: <i>River_Hsu</i>	
Size A4	Project Name 1015P		Rev 1.0G
Date: Saturday, February 06, 2010		Sheet 40 of 42	



<Core Design>

ASUS		Title : load switch	
ASUSTek Computer INC		Engineer: Joy_Zhou	
Size	Project Name	Rev	
C	1015P	1.0	
Date: Saturday, February 06, 2010		Sheet 42 of 42	

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